Patterning of Electrical Circuits on Fluidic Assembly Microtiles

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Abstract

As an alternative to pick-and-place assembly techniques, recent research has lead to the development of microelectro-mechanical systems (MEMS) components that assemble spontaneously in fluid [1-3]. These efforts have relied heavily on surface-energy minimization and therefore work best when components are assembled by vertical stacking to obtain a product with multiple layers. Our research provides an alternative method for interfacing MEMS components assembled in fluid, which involves horizontal (in-plane) assembly. Our previous work has produced silicon microtiles with mechanical latches that can be manipulated by controlling local fluidic forces in a microchamber [4]. The goal of this research was to demonstrate electrical connection between tiles in a single plane. This was achieved by patterning tiles with gold electrodes so that their tops and sidewalls had a continuous covering of conductive material. The result of this research is a novel method for the electrical interfacing of fluidically-assembled MEMS components.

Background

Past research includes fabrication and testing a series of latching silicon microtiles of varying sizes that can be controlled and assembled in a microfluidic channel. The microtiles are manipulated by controlling the fluid flow through a polydimethylsiloxane (PDMS) microchamber with off-chip valving. The tiles are fabricated from a silicon-on-insulator (SOI) wafer using photolithography and a deep ion etch through the top silicon layer, then released from the wafer by etching the oxide using a 49% hydrofluoric acid (HF) solution.

Fabrication

We developed a fabrication method to pattern gold electrodes on 500 μm square by 30 μm high silicon microtiles. Electrode fabrication began prior to HF release, and included evaporation followed by photolithography processes, finally leading to a chemical etch of the metal to form electrodes on the tops and sides of tiles. A wet etch was chosen instead of a lift-off technique to avoid leaving unwanted metal in the trenches between the etched tiles. The consequence of residual metal between tiles would have been either damage to electrodes or no tile separation after release, both results rendering our tiles useless for in-plane fluidic assembly.

Because gold is reluctant to adhere to silicon, a 15 nm chromium adhesion layer was deposited using an electron-gun evaporator, followed by the 80 nm gold layer. After evaporation a thick (35-40 μm) layer of AZ-4903 positive-tone photoresist was spun to cover and fill the gaps between tiles. The resist was removed around electrodes using a two-step exposure and development process (Figure 1). The first exposure patterned the electrodes on the tiles.

During the first development it was necessary to under-develop the electrode pattern, with the purpose of leaving some resist to be removed during the second development. During the second exposure, the trenches between tiles were heavily exposed. A second development removed all resist between the tiles, leaving only sidewall coverage as required for the electrical connections between tiles. A wet etch of both gold and chromium removed all unwanted metal from the silicon.

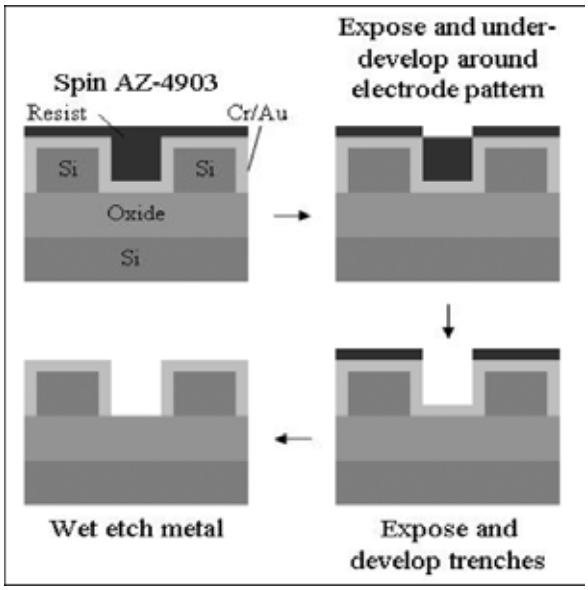

Figure 1: Diagram of two-step exposure and development process for patterning electrodes.

Without this two-step exposure and development process, we experienced either residual photoresist in the trenches between the tiles or overexposure/overdevelopment of the electrodes on the tiles. Finally, tiles were released using 49% HF solution.

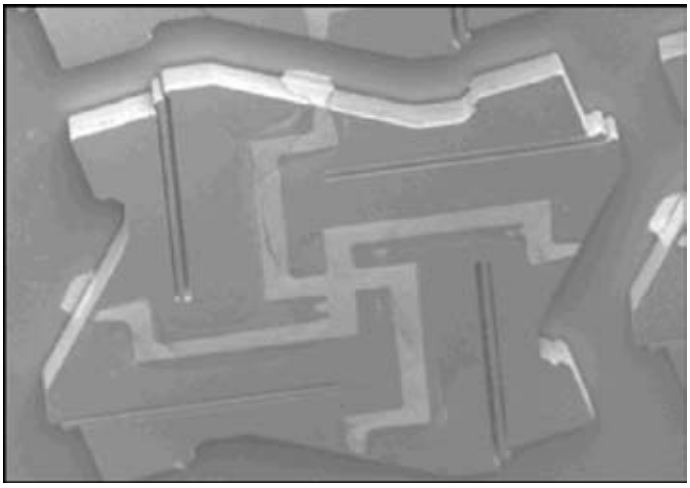

Figure 2: Scanning electron microscopy (SEM) image of silicon tile and gold electrode pattern.

Results

Our fabrication yielded many tiles suitable for electrical testing (Figure 2), though inconsistencies with the electrode pattern did arise, likely caused by variable resist thickness due to edge effects while spinning AZ-4903. Electrical testing using a multimeter probe station verified connectivity across one, two and three-tile circuits assembled in silicone oil on a glass substrate (Figure 3). The tiles were manipulated and assembled using the probe tips (Figure 4).

When compared to similar tests using a non-patterned silicon tile control, electrode-covered tiles yielded a circuit resistance four orders of magnitude smaller. To further characterize our resistance results, we used $R = \rho L/A$ to theoretically calculate circuit resistance, R (Ω). We calculated the theoretical resistance across one tile with chromium and gold wires in parallel to be 4 ohms. Since this value is much smaller than the measured resistances, we assumed that electrode resistance is negligible compared to contact resistances at the tile-tile and probe-tile interfaces. Using this assumption and a least-squares regression, the contact resistances at tile interfaces and for each probe are 880 Ω (0.00792 Ω-cm^2) and 280 Ω respectively.

Conclusion

We fabricated and tested 500 × 500 × 30 μm silicon microtiles patterned with gold electrodes capable of assembling in fluid to form mechanical structures with in-plane electrical connections. By obtaining resistance data across one, two, and three tile circuits, we have verified electrical conductivity across tiles. The results indicate that electrical conduction occurred through planar assemblies of electrode-patterned tiles. Therefore, our fabrication method is capable of producing planar MEMS assembled from individual, microscale components.

Future Work

With the development of our fabrication process, it is possible to obtain simple electric connections between silicon microtiles attached in-plane. Further research will fabricate more complex circuit elements on individual microtiles, enhancing the functionality of systems built from these components.

Acknowledgements

I would like to thank the National Science Foundation as well as the National Nanotechnology Infrastructure Network REU Program for their support of this research. I would especially like to thank Mike Tolley, Mekala Krishnan, Dr. David Erickson and Dr. Hod Lipson, the Erickson Lab as well as the entire Cornell NanoScale Facility staff for their professional help and guidance on this project. Lastly, I would like to thank Dr. Garcia at Cornell for the use of his probe station.

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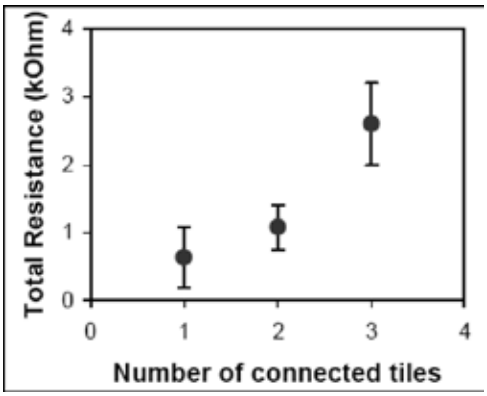

Figure 3: Resistance measurement verses number of tiles. Data points are average measured values. Error bars are minimum and maximum values.

Figure 4: Optical microscope image of resistance measurement across three assembled microtiles.

Development of a Three Degrees of Freedom Atomic Force Microscope

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Abstract

An atomic force microscope (AFM) easily measures forces in one direction. It can be adapted to measure force in the other directions, but it is time intensive and challenging. In this paper, a three degrees of freedom atomic force microscope (3DOF AFM) is presented. Microfabrication techniques are used to design, fabricate, and test a miniature system that can measure forces in three directions with high resolution. Typical applications for the 3DOF AFM are probing nanostructures and studying hard disk drive interactions with the reading head.

Introduction

Atomic force microscopes are used to measure surface topographies. They consist of a cantilever with a tip at the end. A laser beam deflects off the end of the cantilever and into a detector. The detector measures the deflection of the laser beam to find the displacement of the tip as it moves across different surface topographies [1, p. 1614]. AFMs typically measure forces with one degree of freedom, which is in the x direction. The y and z directions are obtainable; however it is time intensive and challenging. A three degree of freedom atomic force microscope can measure forces in all directions.

In order for this to occur, the 3DOF AFM device has to be compliant in all three directions. Compliancy is measured by a low κ value, which is calculated using a finite element simulation software called ANSYS. Figure 1 is depicting the movement of one of the devices in the x direction. This device is made of one vertical thick vertical beam (20 μm) and two thin cross beams (varying between 2 μm or 3 μm). Applications of a 3DOF AFM would be the manipulation and probing of nanostructures, studying hard disk drive interfaces, and understanding nanoscale friction and adhesion forces.

The main objective of this research was to use current microfabrication techniques to design a fabrication process by optimizing both the lithography and process steps in order to fabricate a free standing miniature system that can measure forces with three degrees of freedom.

Experimental Methods

In this research, we developed a fabrication process for free standing micro machines, specifically a three degrees of freedom atomic force microscope. The devices varied from having two cross beams to one beam, the beam thickness varied from 2 μm to 3μm, and the angle between the beams varied from 4° to 10°. Various techniques were used throughout the fabrication process.

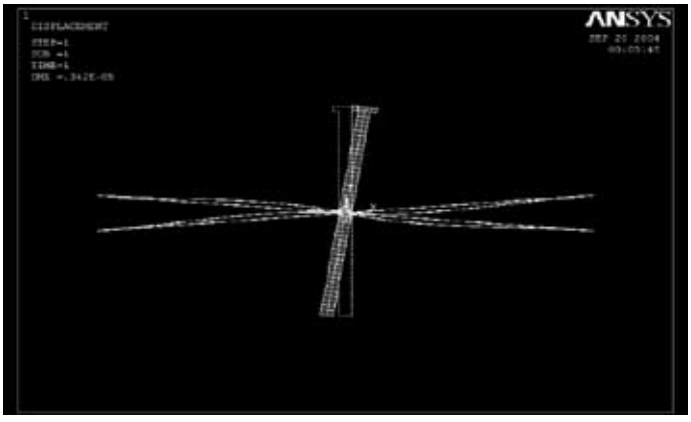

Figure 1: Depiction of the device movement in the x direction from ANSYS.

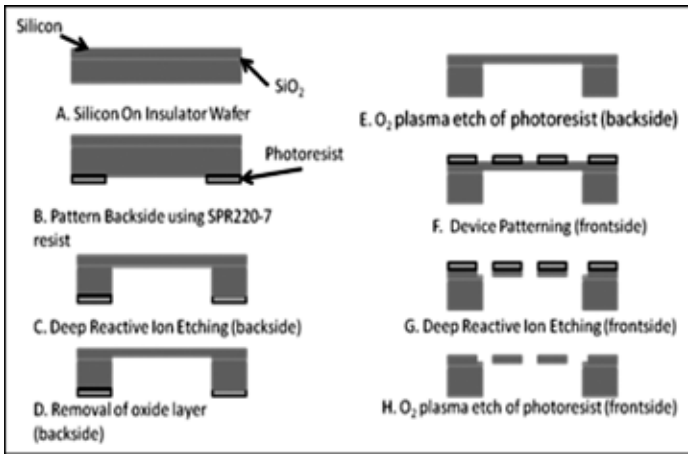

Figure 2: Schematic of the fabrication steps used to fabricate the free standing devices.

Figure 2 is a schematic showing the steps of the fabrication process. The process begins with a silicon-on-insulator (SOI) wafer. 10 m thick SPR220-7 photoresist is used to pattern the backside of the wafer. The first step of the process was to optimize lithography techniques. In order to optimize the lithography process, modifications had to be made due to the resist thickness. The first modification was to use the multiple exposure feature on the Karl Suss MA6 to prevent resist bubbling. The second modification was to skip the post exposure bake to prevent resist cracking. Deep reactive ion etching (DRIE) was used to etch the backside up until the oxide layer. The oxide layer was wet etched using a buffered oxide etch. The frontside mask was then aligned with the backside mask using the MJB3 for device patterning. DRIE is used to etch the frontside the whole way through the wafer. This resulted in free standing devices that were approximately 20 μm thick.

Future Work

We will further develop and modify the fabrication process in order to obtain a higher yield. After the devices are successfully fabricated, they will be mounted to a probe and tested in a FIB SEM. The displacement will be measured and multiplied by the spring constant, κ, (which was previously calculated in ANSYS) to find forces with three degrees of freedom of nanostructures, specifically nanowires on a silicon substrate.

Conclusions

Lithography techniques were optimized and a fabrication process was developed, but not to 100% accuracy. All of the 3DOF AFMs broke during the fabrication process; however we were able to fabricate some 2DOF AFMs. This shows that the fabrication process was successful but had a low yield. Minor modifications have to be made to the fabrication process in order to obtain a higher yield. Figure 3 is one of the 3DOF AFM devices etched 10 μm into a silicon wafer. Figure 4 shows an SEM image of one of the free standing 2DOF AFM devices that were fabricated using the proposed fabrication process.

Acknowledgements

The National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program, National Science Foundation, The Pennsylvania State University Center for Nanotechnology Education and Utilization, and the Nanofabrication Staff. I also want to give a special thanks to my mentor Amit Desai, and my principal investigator Dr. Aman Haque, who are both from the Department of Mechanical and Nuclear Engineering at The Pennsylvania State University.

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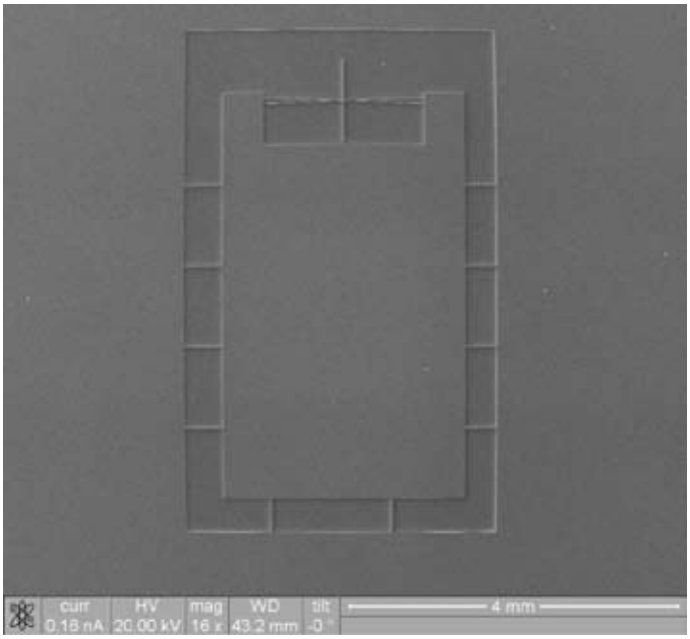

Figure 3: SEM image of a 3DOF AFM (not free standing).

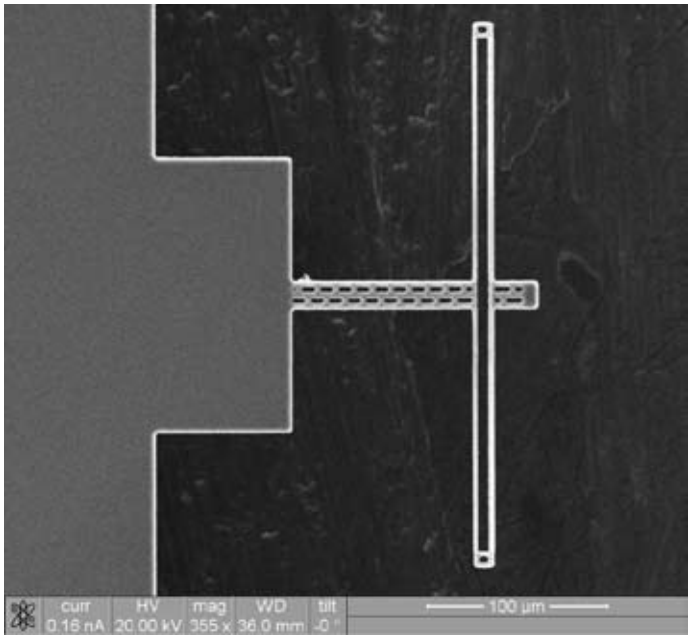

Figure 4: SEM image of a free standing 2DOF AFM fabricated using this fabrication process.

Fabrication of Active Probe Structures for Atomic Force Microscopy

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Abstract

The atomic force microscope (AFM) launched a wide variety of applications ranging from life sciences to metrology after its invention in 1986. However, current applications are limited by several aspects of the conventional AFM technology, which uses a passive cantilever probe and typically slow and bulky piezoelectric actuators. The relatively slow piezoelectric actuators limit the attainable imaging speeds, and the complex cantilever dynamics makes the extraction of quantitative material property characterization difficult. This project addresses these issues by introducing a new probe structure for the AFM. This new probe has a sharp tip placed on an active, electrostatically actuated, micromachined membrane with an integrated displacement sensor. The membrane itself and the diffraction grating form a small phase sensitive optical interferometer for displacement detection. The project focuses on the fabrication of this probe and the experimental results obtained from the fabricated devices. Lift-off process and membrane deposition mainly involve lithography and metallization to fabricate the devices. The devices are then analyzed after being released in the critical point dryer. These results include applications such as fast tapping mode imaging, which utilizes the electrostatic actuator, and time resolving interaction force imaging, which utilizes the well-behaved dynamics of the device.

Introduction

Since its invention, the AFM has found a wide variety of applications ranging from life sciences to metrology. Moreover, AFM is one of the most widely used tools in nanotechnology. For example, applications in physics and chemistry are important for surface property characterization such as stiffness. In biology and life sciences, AFM also can be used in force spectroscopy for drug discovery and ***in vitro*** cell imaging. In engineering and nanosciences, sample information can be obtained by surface roughness analysis and process quality control.

Atomic Force Microscope

The various components of the AFM working together are what enable such diverse applications. A typical AFM has; 1) a micro-cantilever probe, 2) optical lever detection, 3) the piezoelectric tube, which is also the scanner, and 4) the controller. The probe acts as a force sensor, and the cantilever has a very sharp tip with diameter of 2-50 nm. The optical lever detection is used to determine the position of the probe by the photo detector sensing the laser reflected off the cantilever. The piezoelectric tube moves the sample or the probe in x-y-z direction. The controller keeps the cantilever deflection constant through feedback control while the probe scans the sample locally.

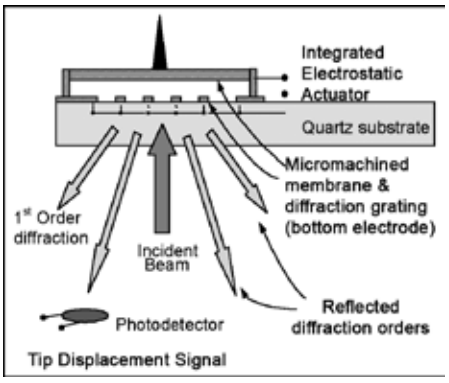

Figure 1: FIRAT probe structure and diffraction based optical interferometric detection.

Current applications are limited by some aspects of the conventional AFM technology, which uses a passive cantilever probe and typically slow and bulky piezoelectric actuators. The relatively slow piezoelectric actuators limit the attainable imaging speeds, and the complex cantilever dynamics makes the extraction of quantitative material property characterization difficult. To tackle this issue, a new probe structure called the force sensing integrated readout and active tip (FIRAT) was introduced.

This new probe has a sharp tip placed on an active, electrostatically actuated, micromachined membrane with an integrated displacement sensor as illustrated in Figure 1 [1]. The membrane itself and the diffraction grating form a small phase sensitive optical interferometer for displacement detection [1]. So the interferometric detection is more sensitive than the optical lever detection of conventional AFM, and the electrostatically actuated membrane is faster than the piezoelectric tube. In order to validate such functionalities of the FIRAT probe, it first has to be fabricated and then analyzed through various experiments.

Experimental Procedure

The fabrication of the FIRAT probe was carried out in the Microelectronics Research Center. We used a 4-inch quartz wafer on which to fabricate the probes. The process began with surface preparation of the wafer by ultra-sonication in acetone for 15 minutes and then in methanol for 15 minutes. Finally, the surface was ready after oxygen plasma cleaning using Plasmatherm reactive ion etching (RIE). Lithography, using the mask aligner,

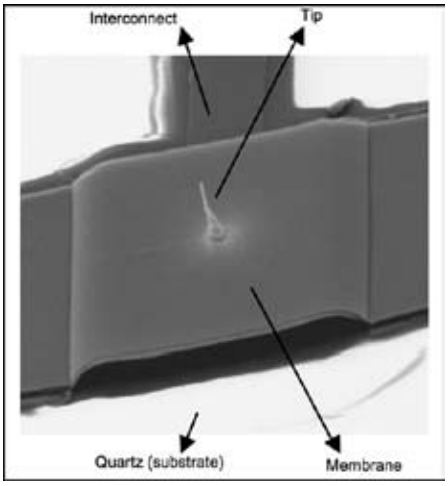

Figure 2: Image of fabricated FIRAT probe. Fingers, not shown, are under the membrane.

resulted in finger patterns. The lift-off process was then carried out to make 0.120 μm Al fingers, which were deposited using the e-beam evaporator. Next, through lithography, a sacrificial layer of about 2.5 μm thick was formed over the Al fingers in order to deposit the Al membrane.

The membrane, which had a thickness of approximately 0.8 μm, was deposited using the DC sputterer. Lithography was carried out again to perform wet etching using aluminum etchant to define the structure. After the ME dicing machine cut the wafer into several probe devices, they were released under photoresist stripper and then in the critical point dryer. A sharp tip, with a diameter of about 50-100 nm, was installed on the membrane of one of the devices using the focused ion beam tool. The final product of such a device is shown in Figure 2.

Results and Conclusions

We were able to successfully fabricate the FIRAT probes. We checked and confirmed the progress of the fabrication by taking images using a digital microscope, and gathering data using a non-optical profilometer at different intervals during the process. Similar probe devices were analyzed using the Wyko optical profilometer to confirm the fabrication of the completed structures. Using the experimental setup in Figure 3, several experiments were conducted on earlier probes, which are similar to the devices that we fabricated [1]. The time resolved integrated force (TRIF) imaging experiment demonstrated that the FIRAT probe was able to characterize stiffness and stickiness of selected samples [2].

The experimental data showed that the membrane only deflected when the probe contacted a hard material sample. However, for a soft material sample, both the membrane and the sample deflected. Thus, the softer material took more time to achieve peak contact force compared to the harder material. The amount of force required for the probe to retract from the sample determined the stickiness. In Figure 4, the fast tapping mode imaging experiment showed that the FIRAT probe was able to track the sample better than a typical cantilever at higher imaging speeds – line scan rates of up to 60 Hz [1]. These results along with other experimental data have shown great promise for the new probe, and were used to explore the extent of its functionalities.

Future Work

Although the current fabrication process does make the production of the probes simple, the probes still cannot not be commercially reproduced. The next step of this project is to design a process to enable mass installment of tips on the probes. This would make the mass production of such probes possible and facilitate the start of commercial production.

Acknowledgments

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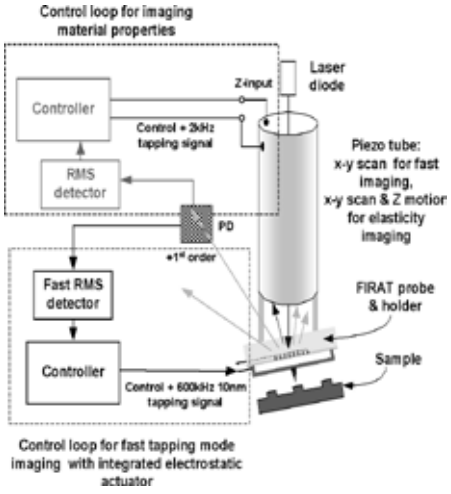
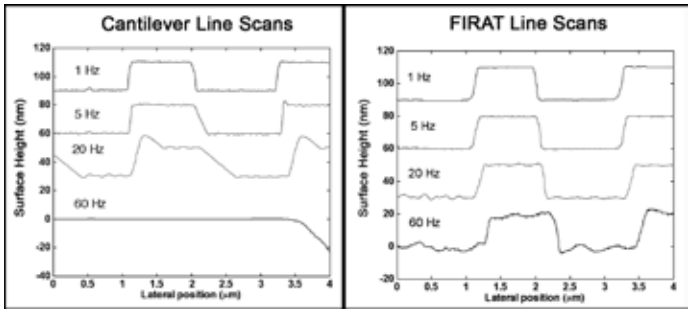


Figure 3, right: Experimental setup integrating the FIRAT probe with commercial AFM system.

Figure 4, below: Line scans of sample at different imaging speeds for each probe.



Characterization of the DRIE Process for ETWI for Piezoresistive Inertial Sensors

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Abstract

Electrical through-wafer interconnects (ETWI) are often integrated with inertial sensors for harsh liquid environment applications. Devices with metal interconnects are very susceptible to corrosion in aquatic environments. An alternative approach is to form highly doped, conductive polysilicon through the wafer from the back side (unexposed to harsh environments) to the front side of the device's chip. ETWI technology requires etching through the wafer. This places a high demand on the through wafer etch profile, critical dimension control, and feature size dependent etch rate (etch lag). On test structures, we measured the sidewall profile and etch rate as a function of several etch parameters (etch cycle time, platen power, current power, C_4F_8 flow, etc). In addition, we assessed practical methodologies for handling the wafer during the etch. The objective of this project is to use statistical design of experiment (DoE) to optimize the deep reactive ion etch (RIE) recipe for through wafer etching and test wafer bonding for through wafer via formation. From the development of electrical through wafer interconnects, more reliable sensor devices can be fabricated for studies in hydrodynamics in harsh environments in addition to a plethora of other applications.

Introduction

We began by optimizing a baseline recipe using STS-HRM (Surface Technology Systems). Then, we used those results to develop a reliable method for through wafer etching. STS-HRM is based on the Bosch method, which uses a process that alternates between the etch gas (SF_6) and the deposition gas (C_4F_8). Moreover, etching occurs by two mechanisms: a chemical process in which fluorine from the plasma bonds with the silicon atoms and becomes a volatile gas, and by a physical process in which the dluoride ions bombard the surface, sputtering the material away. Under proper tuning, the Bosch method achieves an anisotropic (downward direction) etching profile because of the alternating etch passivation cycles. The objective of this optimization was to achieve the following conditions: very straight walls, no grass, and small scallops. However, our major challenge for through wafer etching using STSHRM was thermal management due to backside helium (cooling gas) release, and due to photoresist burning.

As a result of etching completely through the wafer, we lose the helium that is located beneath it; hence, we lose the uniformity of the etch across the wafer, and the cooling that we need in order to prevent the photoresist from burning. Therefore, the single wafer was substituted with a polymer-bonded pair of wafers.

Experimental Procedure

The preparation of the wafers for etch optimization was as follows: spinning 3 μm SPR 220-3 positive photoresist on an SVG coater track; then, a pattern was formed by exposure using a Karl Suss MA-6 i-line mask aligner. The wafers were then developed in LDD 26W developer. The STS-HRM etcher was used for the experimental etch matrix.

Based on "Smooth Shallow Template" (Dep_{time} = 2s; $Etch_{time}$ = 3s; Throttle $Valve_{dep}$ = 15%; Throttle $Valve_{etch}$ = 12.5 %; C_4F_8 flow = 100 sccm; SF_6 flow = 400 sccm; P_{source} = 2500W, P_{platen} = 45 W, Electromagnet - $Etch_{main}$ = 1 A; Electromagnet - $Delay_{time}$ = 0 s), we selected six parameters to optimize: platen power, etch cycle time, deposition cycle time, pressure, C_4F_8 flow, SF_6 flow. We maximized and minimized the ranges and etched twelve wafers with different recipes. Following the cleaving, we proceeded to examine the samples under scanning electron microscope (SEM).

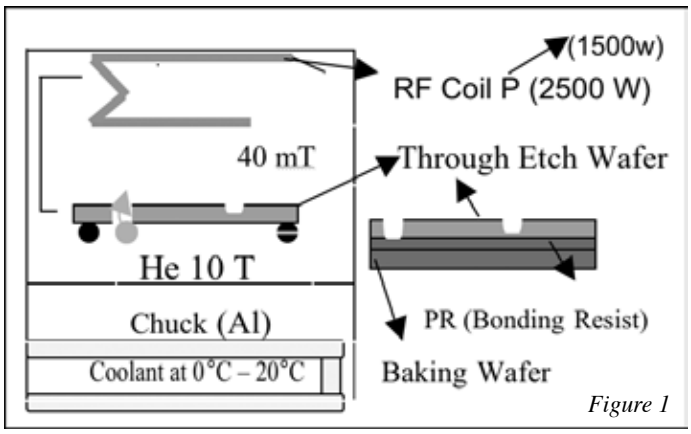

Figure 1

In order to complete a through-wafer etch, a backing wafer was polymer bonded to the through-etch wafer to prevent helium from escaping and to add structural support. First, 10 μm SPR 220-7 photoresist was spun onto the through-etch wafer and 0.5 μm oxide was placed on the backing wafer. Furthermore, 2 μm SPR 3612 photoresist was used as the bonding polymer in between the wafers (Figure 1). Then, both wafers were placed on a 90°C hot plate for 7 minutes with a weight on top. Afterwards, we tested their bond in a vacuum for 5 minutes. Then, we used STS-HRM ("Smooth Shallow Template"), but we lowered the coil power down to 1500 W, because it was discovered that the source power was the principal factor in overheating the wafer. Hence, this reduction in power to 1500 W enabled the masking resist to survive the etch. Finally, we separated the wafers by soaking in acetone for approximately one hour.

Results and Conclusions

In addition, we can conclude that based on the optimization experiment in STS-HRM, reducing the thermal load by decreasing the source power was the key to bonded wafer through etching. Moreover, a wafer-to-wafer polymer bonding technique and a release method were developed for successful through wafer etching in the high rate STS-2 machine.

Future Work

In the future, we could explore new methods for through wafer using aluminum as an etch stop. Moreover, we could set the interconnects through the device's chip and conduct tests in harsh environments.

Acknowledgements

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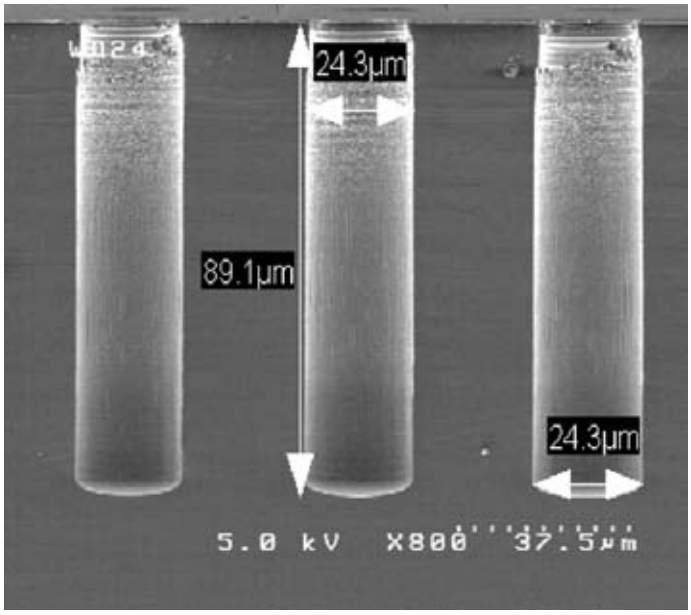

Figure 2, top: We observed very straight and vertical walls, no grass formation, and negligible scallops.

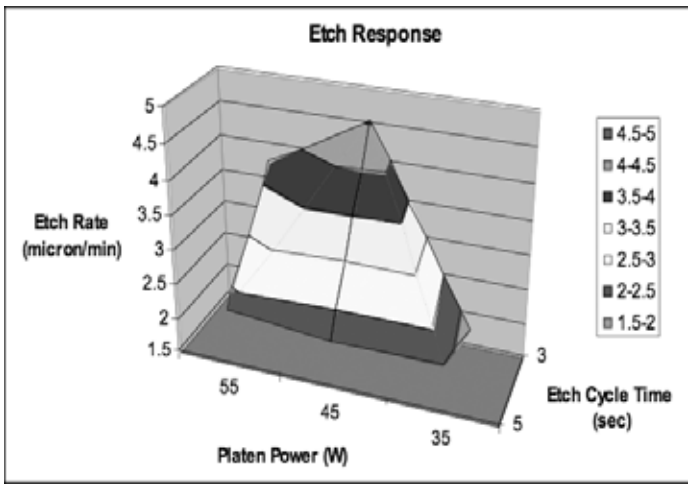

Figure 3, middle: The etch rate achieves 4.5 µm/minute.

Figure 4, bottom: The computer lights passing through the etched vias in the silicon wafer.