Nonvolatile Memory with Multi-Stack Nanocrystals as Floating Gates

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Abstract

Nonvolatile memory technologies are focusing on devices with longer retention, faster read and write, higher bit density, improved endurance, and low-voltage program/erase characteristics. Nanocrystal (NC) memories are promising for realizing high-density nonvolatile storage with the inherent advantage of low-voltage operation [1]. Recently carbon molecules in the form of fullerenes (C_{60}), known as "bucky balls," also have been incorporated in non-volatile memory devices [2] with its advantages of mono-disperse nature and molecular size. In this project, various memory structures with self-assembled multi-stacked gold, platinum, and C_{60} nanocrystals as floating gates have been fabricated and characterized. In two-layer nanocrystal structures, the C_{60} bottom layer acts as an additional barrier to prevent charge back-tunneling from the upper layer, improving retention time without a commensurate penalty in program time. The upper nanocrystal layer functions as additional charge storage to provide sufficient memory window.

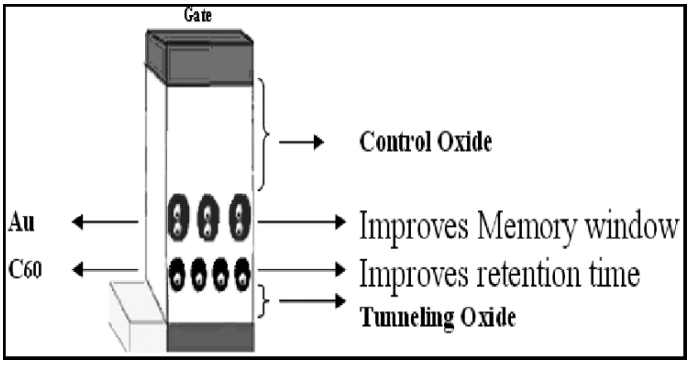

Figure 1: Schematic of the double-layer nanocrystal memory.

Introduction

Figure 1 shows the cross section of a double-layer nanocrystal memory device. By applying enough positive bias across the gate, electrons will quantum-mechanically tunnel through the thin tunneling oxide. If the lower-layer nanocrystal is designed so that it is energetically unfavorable for charge storage due to its small size, electrons will step through the lower nanocrystal layer, and get stored in the second layer nanocrystal. After taking away the applied potential, the energy penalty for electrons in the second layer to tunnel back into the first layer is larger enough, again due to the large charging energy associated with the small size. The first-layer nanocrystal acts as a part of tunneling barrier to provide prolonged retention time. The same concept applies to the hole storage when negative bias is applied. Charging nanocrystals with electrons and holes can require different gate biasing due to different properties of nanocrystals, which also contribute to different retention time characteristics.

The goal was to engineer the best structure such that one can obtain a memory device with an optimal memory window and retention time. This required the optimization of the tunneling oxide thickness, nanocrystal diameter and the choice of a nanocrystal material.

Experimental Procedure

P-type wafers with a doping level of 10^{15} cm^{-3} were used in this study. The device isolation was achieved by the local oxidation isolation (LOCOS). 2-3 nanometers of tunneling oxide was grown on the active region in a diluted oxygen ambience using an atmospheric-pressure furnace. Each wafer was named separately.

Sample 1 (S_1) was the control device without any floating gate, sample 2 (S_2) had a single-layer gold (Au) nanocrystal as a floating gate, S_3 had a double-layer Au nanocrystal floating gate, S_4 had a single-layer C_{60} nanocrystal floating gate, S_5 had a double-layer C_{60} and Au nanocrystal floating gate, and S_6 had the same structure as S_5 but with a thinner thickness of tunneling oxide.

The Au nanocrystals were deposited through e-gun evaporation while the C_{60} nanocrystals through the thermal evaporation. For those samples with double-layer nanocrystals, 2-3 nm of evaporated silicon dioxide (SiO_2) was inserted between two layers. After the floating-gate formation, 20-30 nm of control oxide was deposited through a plasma-enhanced chemical vapor deposition (PECVD), followed by chromium and aluminum evaporation as the control gate. Finally the control gate was patterned to finish the device fabrication. The device was now measured, and memory window and retention time for different configurations were compared.

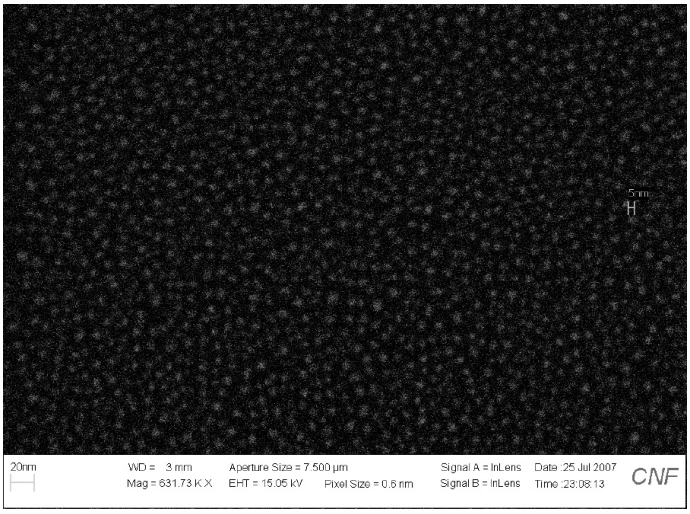

Figure 2: SEM image of Au nanocrystals on SiO_2 surface.

Results and Conclusions

After 1.2 nm Au deposition on the tunneling oxide, the minimization of local energy at the Au/SiO_2 interface reshaped the thin film into discontinuous and spherical Au nanocrystals, as shown in the scanning electron microscopy (SEM) image (Figure 2). The diameter of each nanocrystal was about 5 nm.

To measure the memory window, we performed multiple capacitance-voltage (CV) sweeps from inversion to accumulation and back again. The observed hysteresis of the CV curves indicated memory effect through charge storage. Figure 3 represents the memory window obtained from a double-layer C_{60} and Au floating gate.

We then measured the retention time for each configuration, and as demonstrated in Table I, we compared the values to obtain the optimal configuration for a memory device. Based on the results we concluded that double-layer nanocrystal floating gates with C_{60} as the bottom layer and Au as the upper layer would give the best memory device in terms of memory window and retention time. Since mono-dispersed C_{60} has a diameter of about 1 nm, it performed best in blocking back-tunneling of electrons and holes from the upper layer to the channel in this project.

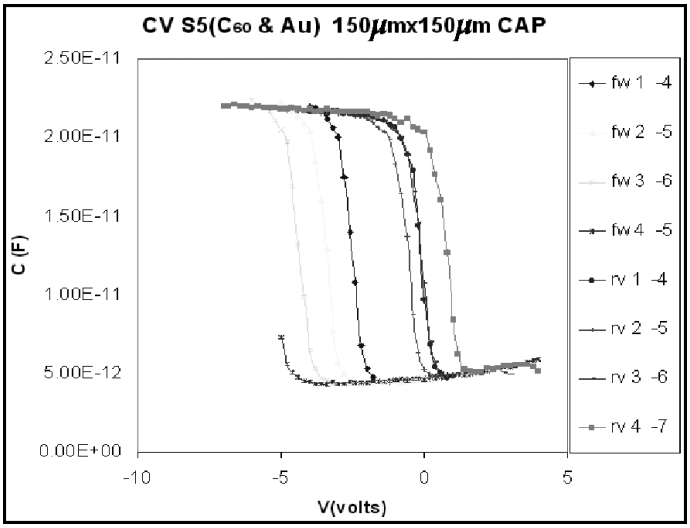

Figure 3: Memory window for a double-layer C_{60}/Au NC memory.

Future Work

More tests will be performed to study the behavior of these memory devices under short-pulse program/erase operations. The retention time will be further improved by incorporating high-κ material as the tunneling dielectric. Finally, the control oxide thickness can be scaled to eliminate short channel effects in the sub-micron gate-length devices.

Acknowledgements

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References

[1] Hanafi, H.I.; Tiwari, S.; Khan, I. , "Fast and long retention-time nano-crystal memory," Electron Devices, IEEE Transactions on Volume 43, Issue 9, Sept. 1996 Page(s):1553-1558.

[2] Hou, Tuo-Hung; Ganguly, Udayan; Kan, Edwin C, "Programable molecular orbital states of C60 from integrated circuits," Appl. Phys. Lett., vol. 89, 253113 (2006).

Run#1 Tunneling oxide = 2.41nm
Run#2 Tunneling oxide = 2.72nm
Voltage sweep (-2 to 5 V)

Sample #	Nanocrystal Layer/s	Run#1		Run#2	
		Mem-win(V)	Reten_t (S)	Mem-win	Reten_t
S1	Control	0	0	0	0
S2	Au	5.8	400	5.4	NA
S3	Au & Au	NA	NA	NA	NA
S4	C60	2.4	240	2.8	250
S5	C60 & Au	3	1100	4.1	5100
S6	C60 & Au	4.7	500	4.4	5000

Table 1: Summary of memory window and retention time.