Epitaxial Growth of Germanium and Silicon Nanowires by Chemical Vapor Deposition

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Abstract

Germanium (Ge) and silicon (Si) nanowires promise to become useful in the further miniaturization of integrated circuits because they allow for precise structuring at scales of 20-50 nm [1]. In order to accurately characterize the electrical properties of nanowires, a necessary ingredient to any semiconductor device integration route, a reproducible process to fabricate them must be established. Chemical vapor deposition (CVD) presents itself as a useful technique in the fabrication of nanowires by utilizing the vapor-liquid-solid (VLS) mechanism, which also allows for the heterogeneous integration of semiconductor nanowires.

Using 2% diluted SiH_4 and GeH_4 in He as precursor gases in controlled pressure and temperature conditions, and with gold (Au) nanoparticles as catalysts for VLS wire growth, epitaxial growth of Ge and Si nanowires on silicon <111> wafers is demonstrated.

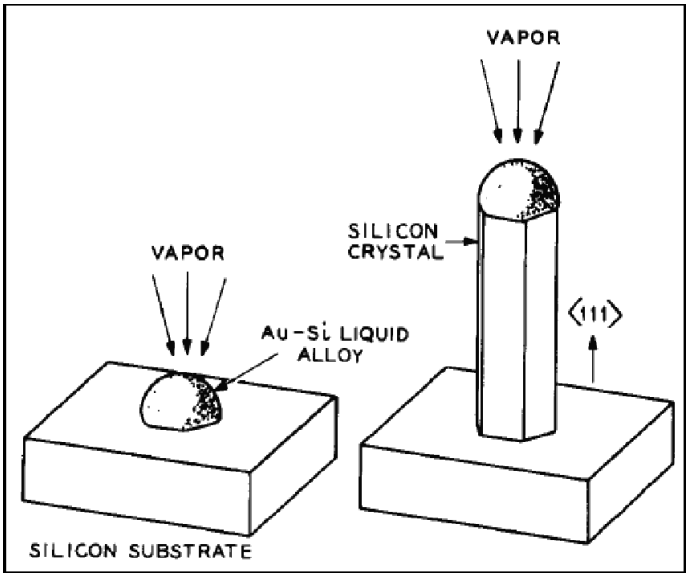

Figure 1: VLS whisker growth [1]. (a) Initial Au droplet absorbs precursor vapor and becomes supersaturated Si-Au alloy. (b) Si from the supersaturated droplet migrates to the crystal lattice of the substrate and forms a silicon whisker in the <111> direction.

Introduction

The VLS growth mechanism of highly anisotropic silicon crystals, or "whiskers," was introduced by Wagner, et al. (Figure 1) [2]. Their study concluded that whisker growth required an impurity and that supersaturated liquid alloy droplets existed on the whisker tips. Subsequent studies have demonstrated reduced whisker sizes down to the nanoscale in silicon [3,4], germanium [5], and III-V compounds [6].

CVD of silicon and germanium nanowires utilizes VLS transport, in which a gold catalyst provides lower dissociation energy (rather than the bare substrate) for the decomposition of the carrier gas, H2, from the precursor, Si or Ge, in the following reactions at the vapor-liquid interface:

$$SiH_4(g) \rightarrow Si + 2H_2(g)$$
$$GeH_4(g) \rightarrow Ge + 2H_2(g)$$

The semiconductor material then diffuses through the droplet, which is liquid at growth temperatures as it forms an eutectic alloy with the Au. Once supersaturated, the semiconductor atoms are incorporated into the crystal lattice at the liquid-solid interface, with epitaxial growth in the <111> direction.

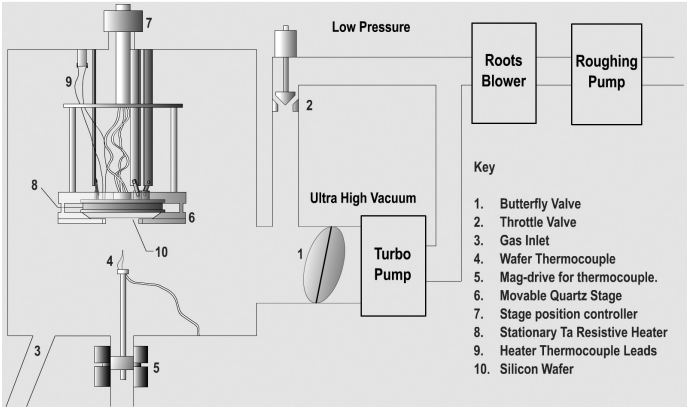

Figure 2: Schematic representation of the CVD apparatus used in the study.

Process

The growth apparatus (Figure 2) used here was a cold wall CVD reactor containing a tantalum (Ta) resistive heater encased in quartz, with operating pressure range of 10^{-8} Torr to 20 Torr. A 1/4 inch gap existed between the wafer and the heater, causing a difference in heat transfer when a precursor gas was or was not present. Thermocouples directly contacting the filaments monitored heater temperatures. Heater voltages and current were also monitored. An unfixed thermocouple measured the wafer temperature.

Silicon <111> wafers were prepared by a 45 second hydrofluoric acid (HF) dip, rinsed, and transferred within 10 minutes to a high vacuum ($\sim 5.0 \times 10^{-6}$ Torr) metal deposition chamber. After depositing a 10Å gold (Au) film, the wafer was transferred into the CVD chamber (approximately 1 hr after HF dip).

Germanium nanowires were produced in a two step process. First, the wafer temperature was raised to 400°-450°C for 5-10 minutes in order for the Au film to coalesce into droplets. The wafer temperature was then lowered within 30 min to a specified temperature, ranging from 230° to 280°C, and GeH_4 was introduced. The reactor pressure was maintained at 10 Torr.

Similarly, silicon nanowires were produced by raising the wafer temperature to 530°-580°C in 60-90 min and introducing SiH_4 into the chamber, maintaining reactor pressure at 10 Torr.

Results

In order to establish Ge wire growth, a series of growths at substrate temperatures of 300°C, 275°C, and 240°C were performed. High temperatures produced tapered wires, a result of the combination of axial and conformal growth. Figure 3 shows the scanning electron microscopy (SEM) data of Ge wire growth carried out at a pressure of 10 Torr and a substrate temperature of ~ 240°C. The measured nanowire growth rate was ~ 1.5 μm/hr, with a nanowire aspect ratio of 33:2.

Si wires were produced at a growth pressure of 10 Torr, with wafer temperatures of 580°C, 550°C, and 530°C. Epitaxial growth was less pronounced than in the Ge growths. Figure 4 shows, at 2 hours, a silicon wire growth maintained at a pressure of 10 Torr and wafer temperature of ~ 580°C. The axial nanowire growth rate was ~ 5 μm/hr, with a nanowire aspect ratio of 40:1. The wires grown at a higher temperature showed a significant surface roughness.

Future Work

The current apparatus separates the heater from the wafer, which results in a wafer temperature dependence on the precursor pressure as well as a large temperature gradient between the heater and wafer. To mitigate these issues, a replacement boron nitride heater will be installed directly contacting the wafer, also allowing for higher wafer temperatures during growth.

Once grown, the nanowires will be deposited onto dielectric wafers, and we will fabricate three terminal, back-gate devices with metal contacts, allowing electronic properties to be characterized.

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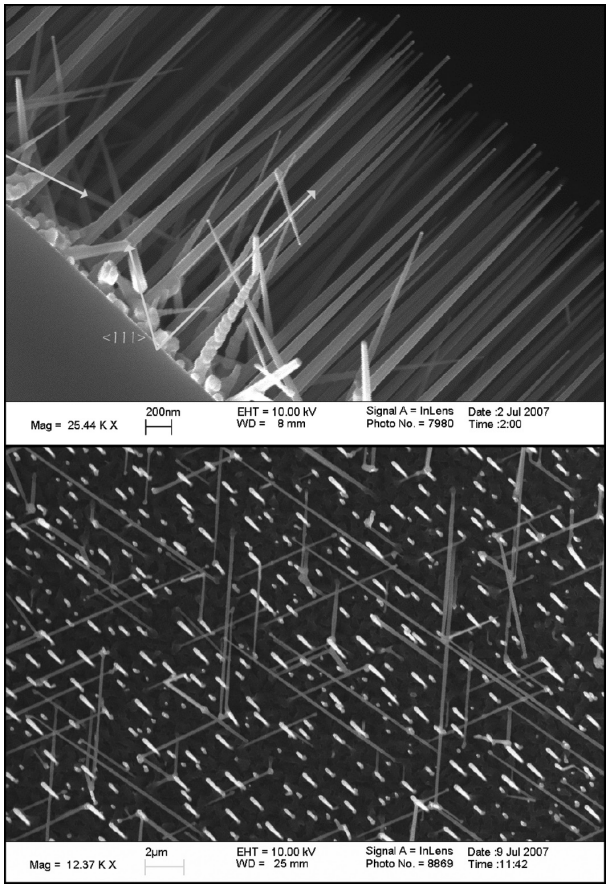

Figure 3, top: Cross-sectional SEM image of showing growth along the three <111> directions, predominately vertical, demonstrating epitaxial Ge nanowire growth on a Si substrate.

Figure 4, bottom: Top down SEM image of silicon nanowires. The three <111> growth directions, aside from the normal to the substrate, can be clearly seen.