

## Deterministic Growth of Silicon Nanowires

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### Abstract

If it were possible to grow nanowires exactly where needed, then devices could be fabricated with fewer processing steps. We are developing a method that enables silicon nanowires to be grown from the  $\langle 111 \rangle$  sidewalls of trenches etched into silicon wafers. The nanowires are grown from a gold catalyst that is selectively plated on n-type wells patterned into the  $\langle 111 \rangle$  sidewalls of the trenches. The goal of this summer project is to develop a process to fabricate these platforms for nanowire growth using the Penn State Nanofabrication laboratory.

Normally, nanowire growth and alignment for devices involves two separate steps, growth and then alignment. These devices' creation relies on where, and how accurately, the wires are aligned. Being able to determine where the wires are grown by creating areas for gold plating eliminates the two step process of growing and aligning.

### Experimental Procedure

This process starts with  $\langle 110 \rangle$  face silicon wafers with 380 nm of silicon dioxide ( $\text{SiO}_2$ ) grown on the surface. After the oxide growth, we performed electron beam lithography on the samples. ZEP520A resist was spun on, and once applied it was  $\sim 400$  nm thick. The electron beam patterned 200 nm lines running perpendicular to the  $\langle 111 \rangle$  flat in the center of the wafer. After creating these lines, the samples were dry etched using reactive ion etching (RIE) to remove the  $\text{SiO}_2$  layer exposed by the lines. Since the resist layer was very thin compared to the  $\text{SiO}_2$  layer, an etch recipe selective to  $\text{SiO}_2$  was created. Varying gas concentrations and bias voltages, the following recipe gave the best results; 50 sccm  $\text{CF}_4$ , 40 sccm Ar, 8 sccm  $\text{H}_2$ , 300 V DC, and an etch time of 20.5 min.

Being able to grow the wires hinges on having the n-type regions in the silicon. Therefore, applying the dopant so it fills the channels is crucial to the process. The best way to accomplish this was by incorporating spinning and vacuum techniques.

The dopant was in the form of a spin-on-glass with 10% phosphorous included. The spin-on dopant was applied at 1000-2000 rpm, allowing it to coat evenly, and placed in a vacuum chamber allowing any air to escape so the dopant could fill in the channels. The sample was then bake at  $100^\circ\text{C}$  for 30 sec and at  $200^\circ\text{C}$  for 5.5 min to remove solvents. Figure 1 shows an etch channel in  $\text{SiO}_2$  that is filled with dopant.

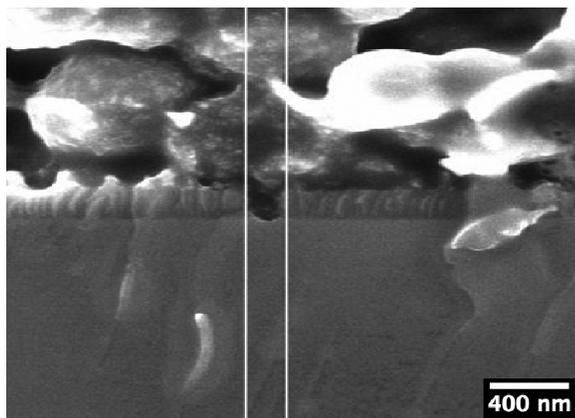


Figure 1:  $\text{SiO}_2$  channel filled with dopant.

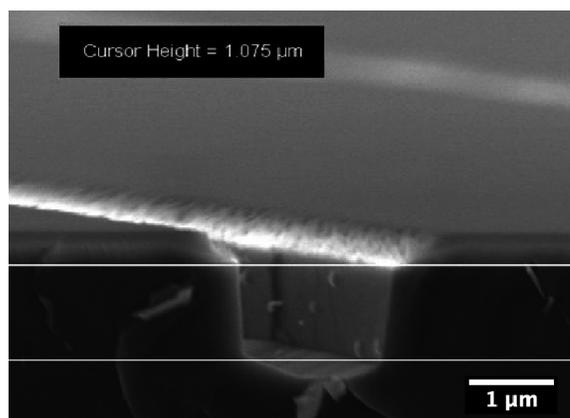


Figure 2: Two minute KOH etched trench.

Diffusing this dopant creates the n-type regions in the silicon needed during subsequent gold plating. A junction depth of 200 nm is desired. After calculations, placing the sample into a furnace for 0.5 hr at 950°C achieved this depth. Placing the sample in a 6:1 ratio of buffered oxide etch (BOE) removed the oxide layer after diffusion.

A masking layer during the future KOH etch was a necessity, and silicon nitride worked adequately. A plasma enhanced chemical vapor deposition system (PECVD) deposited 125 nm of  $\text{Si}_3\text{N}_4$  onto the silicon surface. Samples now went through the photolithography process, using Shipley 1827 photoresist. Lines were patterned 100 nm wide, running parallel with the flat of the wafer. The photoresist was now very thick compared to the nitride, so selectivity was not a very big issue and the etch recipe used for  $\text{SiO}_2$  worked very well. That recipe gave a nitride etch rate of about 60 nm/min, so the etch time was decreased to 3 min.

Etching silicon with KOH at 60°C is slow enough (11 nm/sec) to give a shallow enough trench in a reasonable time (1.5 min). There was now a grid in the middle of the wafer, formed from the n-type regions and the newly etched trenches in the silicon, exposing the areas where the plating of gold occurs. Figure 2 shows a trench etched for 2 min in 60°C KOH bath. The gold plating was on the n-type wells on the sidewalls.

There is a process which causes gold to selectively plate more densely onto these n-type regions [1]. These gold pads were the catalyst used for the nanowire growth step. The nanowires were grown using the vapor-liquid-solid growth mechanism with silane as the silicon precursor gas.

## Conclusions

After growing the wires, scanning electron microscope (SEM) micrographs showed that wires were growing all over the surface. This was because the nitride layer which was supposed to serve as a mask during the gold plating, was no longer on

the surface. We found that the gold had plated on the n-type regions—not only in the trenches, but on the top of the sample as well. Figure 3 shows an image of the n-type regions with wires growing off the surface. The nitride layer disappeared because the sample was placed in a 10:1 BOE for 2 sec. This short immersion completely removed the nitride layer and left the entire surface exposed. The nitride layer possibly had a large amount of hydrogen incorporated, making it etch aggressively in BOE. Even though the image does not show wires growing from the sidewalls, there is no reason not to believe wires were growing there as well.

## Future Work

Future work entails developing a more durable nitride layer so the BOE dip does not strip it off. Also, we need to improve the rinsing techniques after plating the gold so no gold settles onto the surface that is not n-type.

## Acknowledgements

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## References

- [1] “Selective plating for junction delineation in silicon nanowires,” C. M. Eichfeld, C. Wood, B. Liu, S. M. Eichfeld, J. M. Redwing, and S. E. Mohny, *Nano Lett.*, in press.

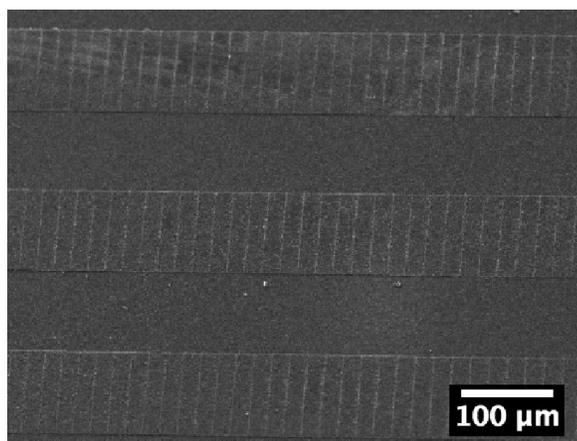


Figure 3: Sample after wire growth.