Investigation of TMAH Release of Stretchable Silicon Networks

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Abstract

The development of stretchable silicon networks is an important step to realizing cost-effective large area electronics. Devices were fabricated using conventional complementary metal oxide semiconductor (CMOS) processing on wafers which were etched into networks of nodes connected by spiral springs and then stretched to desired size and shape. This investigation focused on developing an approach to release these networks following deep reactive ion etching using a tetramethylammonium hydroxide (TMAH) etch on <111> wafers. To achieve effective release of these networks, etching parameters such as etch time and temperature of etchant bath were varied until optimal process parameters such as etch rate and oxide selectivity were determined. The ability to successfully create a device on a standard 4″ silicon wafer and stretch it to a size ten times or larger is important in the implementation of many large area electronics applications, such as structural health monitoring sensors and solar cells.

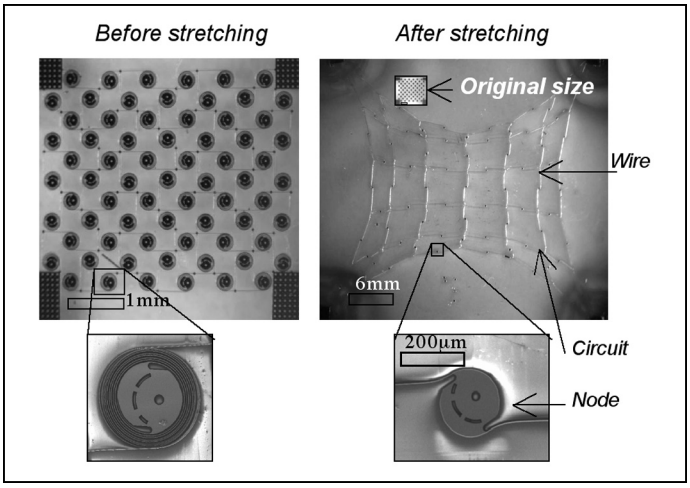

Figure 1: Stretchable silicon network before and after stretching.

Introduction

This research investigated a cost-reducing, consumption friendly fabrication process to release two-dimensional stretchable silicon structures. Eventually, devices or sensors will be placed on individual nodes, in which the spiral springs serve as built-in circuit interconnects for creation of an integrated, robust system as shown in Figure 1.

Previously, stretchable silicon network fabrication required using silicon on insulator (SOI) wafers and employed the xenon difluoride (XeF_2) isotropic dry etch process to release the devices from the substrates. This process was expensive due to the cost of the SOI wafers and inability to reuse the wafers following a single process run. In addition, it was prone to structural problems stemming from pinhole defects particularly in the sidewalls. In response to these consequences, a new wet etch process was employed.

TMAH is a well known non-toxic, anisotropic wet etch solution that was chosen for its ability to etch specific crystal planes at specific rates, its high selectivity to oxide, and for its compatibility with the CMOS process as it does not contain harmful alkali ions [1]. Because TMAH etches the <111> plane at the slowest rate, it can act as an etch stop much like the buried oxide does in the SOI wafer when bulk Si <111> wafers are used.

Device Fabrication

The substrates for this investigation consisted of 4″ diameter, <111> oriented Si wafers which were selected for their compatibility with the TMAH target etch planes. The device fabrication process started with the blanket deposition of a 1.6 μm thick layer of silicon oxide via low pressure chemical vapor deposition (LPCVD). Next, standard photolithography steps were performed. A dry fluorine etch was subsequently used to etch the exposed network pattern in the oxide. Si was then etched using the Bosch deep reactive ion etch (DRIE) process which consisted of an alternating sulfur hexafluoride (SF_6) etch process and a deposition of octafluorocyclobutane (C_4F_8), which served as a protective passivation layer over the etched structures to create a smooth sidewall.

Next, a 2 μm layer of oxide was blanket deposited using LPCVD. A second oxide etch removed the bottom layer of oxide, preparing the wafer for another DRIE. This prepared the Si wafer for the wet etch release. Figure 2 shows the resulting device structure following the second DRIE step. Finally the wafers were subjected to a TMAH bath heated over a hotplate to ensure thorough undercutting of the nodes, spirals, and pads. The bath was closely monitored to ensure a constant temperature and the solution was agitated to help decrease the quantity of hydrogen bubbles, which can disrupt the etching process.

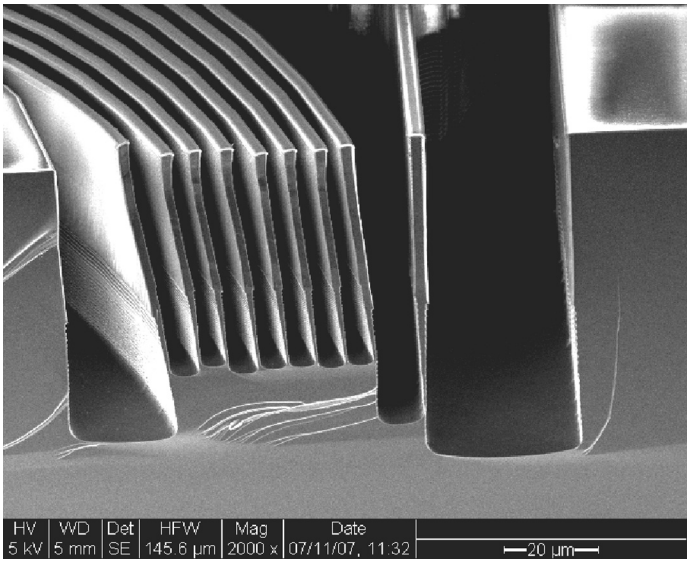

Figure 2: Cross-section of device prior to TMAH wet etch.

Results and Conclusions

Complete structure fabrication was achieved in a clean room environment, and optimal production specifications were determined to successfully release the Si structures from the wafer.

It is well known that planar etch rates are inversely related to the TMAH concentration, thus for optimum results, a 5% TMAH: 95% water bath ratio was used at a temperature of 90ºC [2]. With an optimum etch rate of 1.4 μm/min in the <110> plane, the TMAH etch process time was determined to be 80 minutes to effectively undercut the silicon nodes, interconnects, and pads. However, transferring the networks between liquid and gaseous states proved difficult.

Traditionally, critical point dryers (CPD) are used to reduce the negative consequences of surface tension. However, the stretchable Si structures are delicate, hence they became easily entangled due to the gas flow in the dryer, as shown in Figure 3. This prompted a new investigation directed at successful removal of the structures following the TMAH bath. One solution was found by increasing the distance between the released structure and the substrate during the final DRIE step, followed by air drying the samples after release. Although the substrates still had to be removed from the TMAH solution and thus were subject to some tangling, the networks were nevertheless released without being introduced to the CPD.

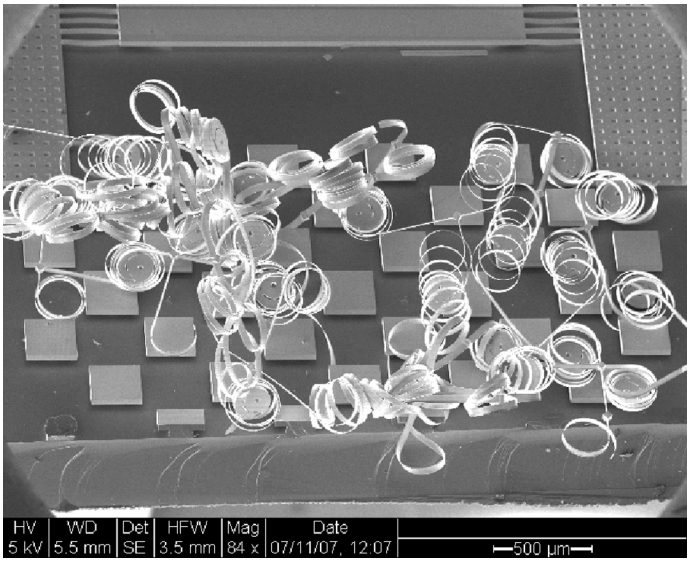

Figure 3: Tangled node network following TMAH etch.

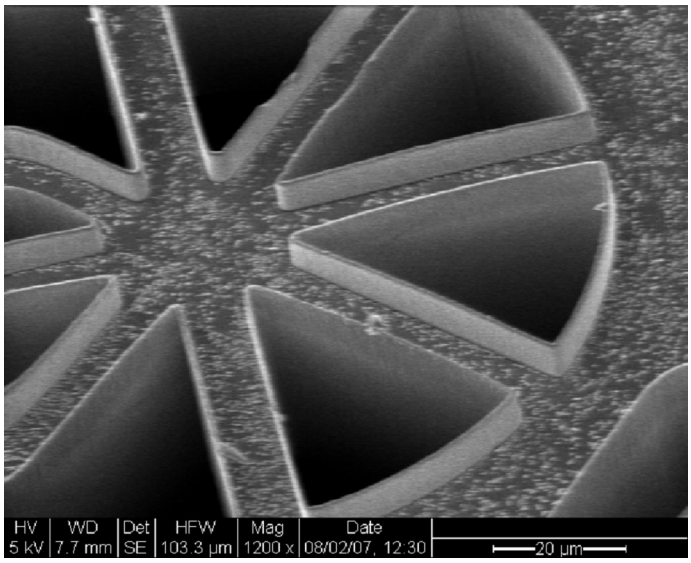

Figure 4: Underside of node showing clean release.

Figure 4 shows a cleanly released node structure. Future work will involve improving this release mechanism. However, we have shown that a cost-effective method to fabricate stretchable silicon networks is viable and important in the implementation of various sensor devices.

Acknowledgements

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[2] Laconte, J., et. al. "Micromachined Thin-Film Sensors for SOI-CMOS Co-Integration". New York: Springer, 2006. p. 17-46.