The Integration of Nanowire Electronics with Top-Down CMOS through Direct Growth

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Abstract:

Nanowires have shown significant potential for future electronic, optical and bio/environmental sensing applications. Here we discuss our efforts to integrate semiconductor nanowires with on-chip micro-scale components by combining the bottom-up nanowire synthesis with top-down fabricated growth sites. Pairs of electrodes were first defined by conventional lithography methods and were used as nanowire growth sites. Gold (Au) nanoparticles with diameters of 20 nm were then deposited on the sample to serve as catalysts during the nanowire growth. We developed a process to successfully isolate the Au nanoparticles on the sidewalls of the electrodes. Tin oxide (SnO_2) and silicon (Si) nanowires were then grown on the samples using the vapor-liquid-solid (VLS) method. After growth, the samples were examined with scanning electron micrograph (SEM) for evidence of controlled nanowire placement.

Introduction:

Nanowires (NWs) are single-crystals with diameters as small as a few nanometers and lengths up to tens of micrometers. The small sizes and excellent material properties of NWs have led to the demonstration of an array of NW-based electronic, optical and bio/environmental sensing devices. Most NWs are grown by the vapor-liquid-solid (VLS) method [1] using nanoparticles as catalysts. In a typical process, the as-grown, haystack-like NWs are processed after growth [2,3], e.g., via solution sonication and random dispersion onto target wafers, where electrical contacting and/or characterization are subsequently performed. However, the locations of the nanowires are not controlled in this approach and working devices have to be designed manually. Instead of following the "bottom-up synthesis first, top-down fabrication next" approach, it may be desirable to grow nanowires precisely and rationally in predetermined device architectures [4]. Direct integration of NW growth into device fabrication will markedly simplify the process flow and allow the access of individual NWs in a parallel fashion. In this research, we attempted to tackle the integration of nanowire electronics by the direct growth of semiconducting nanowires from desired locations on micro-scale components. This approach can potentially eliminate the post-growth processing steps and solve the "position registry" problem for nanowire-based electronics.

Device Fabrication:

A negative photoresist layer, with a monolayer of HDMS serving as adhesive, was applied to a 600 nm oxide substrate, followed by the patterning of experimental designs using photolithography, and pattern transfer to the oxide layer by wet etching, to produce electrode pairs with exposed sidewalls. A thin coat of nickel was then evaporated, followed by the deposition of gold nanoparticles with diameters of 20 nm to serve as catalysts during the nanowire growth. The nickel layer as well as the photoresist layers were removed which isolated the gold nanoparticles on the sidewalls of the oxide. SnO_2 nanowires were then grown from the gold nanoparticles using the well-known VLS method. An array of gold dots was also fabricated using electron beam lithography to demonstrate that silicon nanowires can be grown from controlled locations.

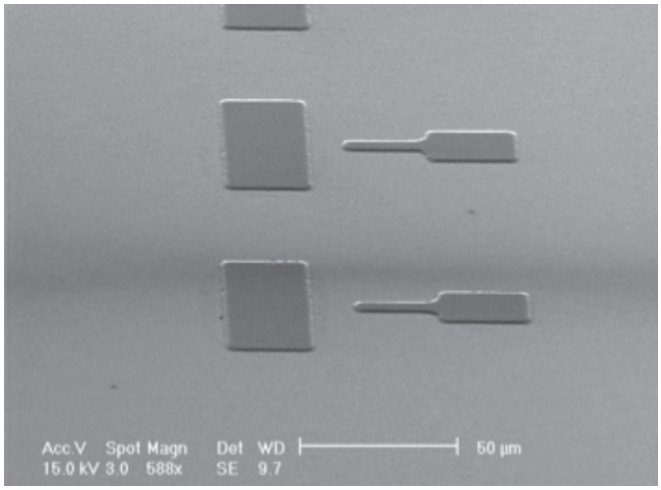

Figure 1: SEM image of two pairs of electrodes before the nanowire growth process.

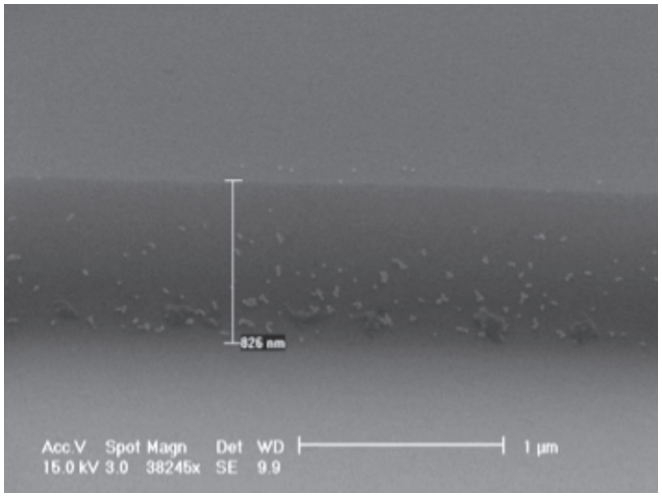

Figure 2: SEM image of Au nanoparticles isolated on the sidewall of an oxide structure.

Results and Conclusion:

Figure 1 shows pairs of micro-scale electrodes from which nanowire growth would be initiated. In Figure 2, 20 nm gold nanoparticles were successfully isolated along the sidewalls of the oxide structures. Since gold serves as a catalyst for SnO_2 nanowire growth, the isolation of gold nanoparticles suggested that localized growth was possible. Indeed, localized growth of SnO_2 nanowires from the micro-scaled electrodes was achieved as shown in Figure 3; however, it was very difficult to visibly conclude if nanowires actually connected any components because of the large number of nanowires that were present.

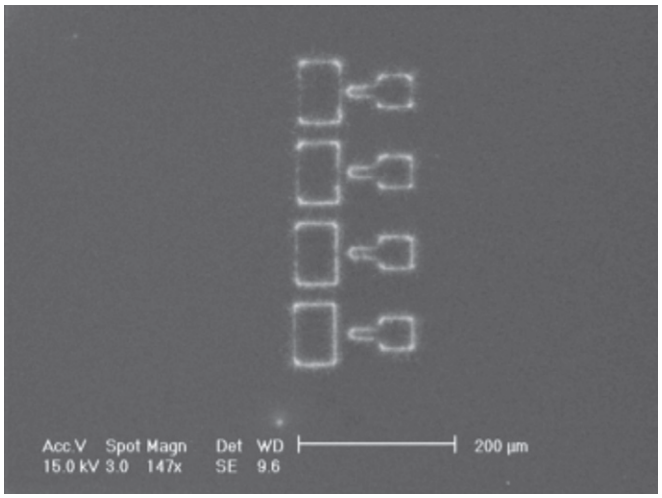

Figure 3: SEM image of localized growth of SnO_2 nanowires from the oxide structures.

To unambiguously verify the controlled growth of nanowires, we performed another experiment in which Si nanowires were grown from gold dots placed in desired locations by e-beam lithography. The results are shown in Figure 4 and clearly demonstrated the one-to-one correspondence between the nanowires and the gold dots, and the controlled growth of Si nanowires from pre-defined catalyst sites.

In conclusion, the findings of catalysts isolation, localized nanowire growth, and controlled growth of Si nanowires from pre-defined locations provided strong evidence that integrating semiconducting nanowires with on-chip micro-scale devices can be done with the appropriate conditions.

Future Work:

The growth process for SnO_2 and Si nanowires needs to be further optimized for experimental conditions. Ideally, one nanowire will be grown from and bridge a pair of electrodes. This requires further adjusting the catalyst density and electrode design. Epitaxial growth from the sidewalls of the electrodes is also desired and it requires preferential etching of the material to expose the desired surface orientation. These improvements would greatly increase the probability of integrating bottom-up nanowire growth with top-down fabricated micro-scaled devices.

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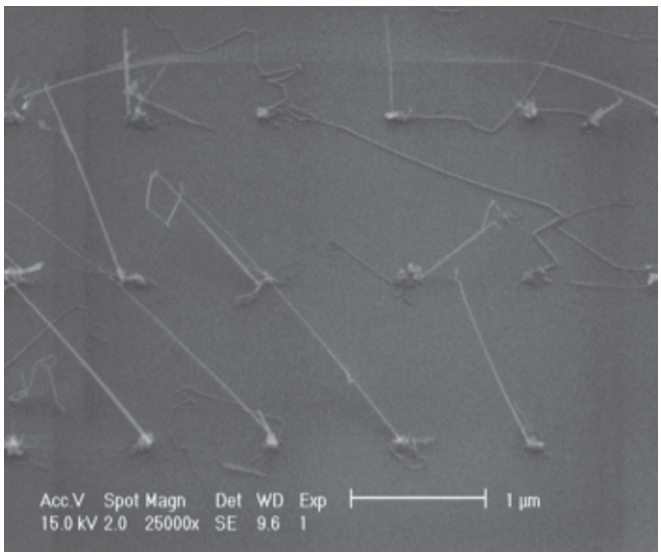

Figure 4: SEM image of controlled growth of Si nanowires from pre-defined Au nanodot sites.