

High- κ Gate Stack for d-DotFET

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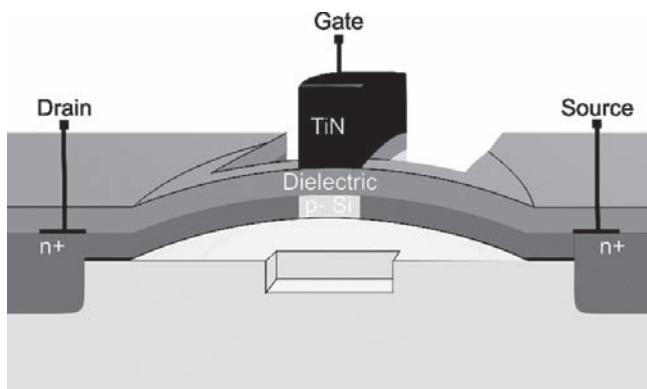


Figure 1: Schematic of the d-DotFET.

Introduction:

The Disposable Dot Field Effect Transistor (d-DotFET) is a collaborative research project, funded by the European Commission, aimed at utilizing a strained silicon (Si) channel in a traditional metal oxide semiconductor field effect transistor (MOSFET) design; thereby achieving a faster transistor. In a strained Si layer, the interatomic distance between atoms is higher than that of normal Si. As a result, strained Si exhibits higher electron carrier mobility than normal Si. In the d-DotFET project, biaxially strained Si is achieved by growing a layer of Si over a pseudo-substrate of silicon germanium (SiGe). Specifically, the silicon is grown over a germanium dot that is later evacuated. However, the nanoscale dimensions of the d-DotFET require gate structures on the scale of 50 nm.

The goal of this project was to create a fabrication process for a high- κ gate stack consisting of 50-100 nm conducting layer of titanium nitride (TiN) and a thin dielectric layer of either silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or gadolinium scandate (GdScO_3).

Experimental Procedure and Results:

The nanoscale dimensions of the gate stack requires that the TiN etching process produces vertical flanks—what is known as an anisotropic etch. Reactive ion etching (RIE) experiments on samples of TiN/ GdScO_3 were conducted using a chlorine (Cl_2) plasma. The samples were prepared

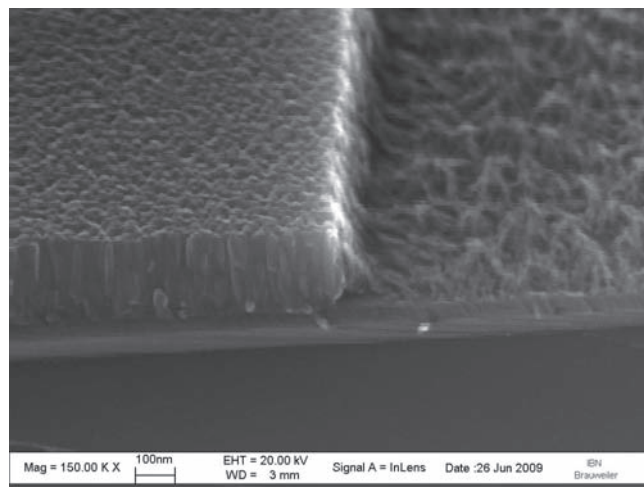


Figure 2: Cl_2 plasma etch of TiN on top of GdScO_3 layer.

by depositing a layer of GdScO_3 on top of a Si substrate, and subsequently sputtering TiN on top of the GdScO_3 layer. As can be seen in Figure 2, a sample etched in a Cl_2 plasma resulted in relatively vertical flanks.

A profilometer was used to test the depth of the etch for increasing etch times on samples of 400/10 nm of TiN/ GdScO_3 . Figure 3 shows the results when using a Cl_2 plasma with a RF bias power of 10 W, an ICP power of 1000 W, at 20°C, with 30 sccm of

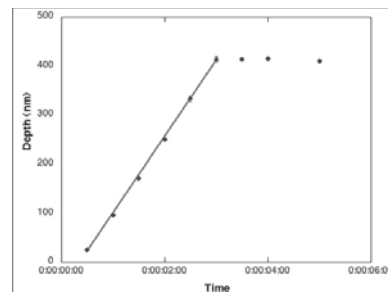


Figure 3: TiN etching with Cl_2 plasma

Cl_2 . The Cl_2 plasma etches TiN at the rate of 150 nm/min. In addition, the plasma stopped well on the GdScO_3 layer, failing to etch the layer after two additional minutes of etching. This indicates a selectivity greater than 30—a very high selectivity of TiN over GdScO_3 .

When etching with Cl_2 , we found that a grass-like layer of titanium oxide (TiO), most likely titanium dioxide (TiO_2),

was left after the etching of TiN. The TiO₂ residue can be seen in Figure 4, where a Cl₂ plasma has etched away ~ 260 nm of TiN from an originally 400 nm layer of TiN. What remains on top is a ~ 170 nm grass layer of TiO₂.

Previous studies on the oxidation of TiN give evidence that the grass layer is composed of TiO₂ [2]. We surmised that the columnar structure of TiN lead to the creation of TiO₂ in between the TiN gaps. Hence, when TiN is etched, the TiO₂ remains as a porous grass-like layer. To further verify that the grass-like layer was titanium oxide, we performed an elemental analysis using an energy dispersive x-ray spectroscopy (EDX) measurement. The measurement was performed on a etched sample of TiN/GdScO₃/Si. The qualitative measurement found the sample to be composed of titanium, oxygen, gadolinium, scandium, and silicon (Ti, O, Gd, Sc, and Si). Hence, we were able to rule out several possible compounds such as titanium chlorides.

We also inferred that the top of the TiN layer had been oxidized, forming a thin layer of TiO₂. This would explain the 20-30 s of inhibition time that occurred when we etched TiN with Cl₂. This was in agreement with prior experiments using SF₆ etching, where there was no inhibition time, and subsequently no grass-like layer remaining after the TiN etch. This was a result of SF₆ etching TiO₂ much more effectively than Cl₂ [3].

One of the goals of this project was to use GdScO₃, a high constant (high- κ) dielectric, in conjunction with TiN. Ideally, the GdScO₃ layer could be etched with a process similar to the one used to etch the TiN layer. As seen previously in Figure 3, Cl₂ is very poor at etching GdScO₃. However, it has been shown that the selective removal of GdScO₃ over Si is possible using a combination of chlorination and water purging [1]. Chlorinated GdScO₃ is water soluble. Hence, it is removed when rinsed with water. The appropriate process is to first expose the GdScO₃ layer to 30 s of a Cl₂ plasma, chlorinating the surface, and then water purge the layer, removing 1-2 nm of GdScO₃ [1].

An experiment was conducted in which a 400/8 nm sample of TiN/GdScO₃ was etched for 3.5 min with a Cl₂ plasma at a plate power of 10 W. The intent of this etching was to remove the TiN layer. Then the sample was etched with a Cl₂ plasma with a plate power of 50 W to chlorinate the GdScO₃. The sample was then water rinsed and the procedure was repeated eight more times for a total of nine cycles. Scanning electron microscope images showed us that the GdScO₃ layer was removed, albeit inhomogeneously. This inhomogeneous removal is the result of a micromasking effect caused by the TiO₂ grass-like layer.

Future Work:

We have identified a process that will etch TiN with the selectivity and anisotropy required at nanoscale dimensions, and identified methods for etching the various underlying dielectrics that could be used in our gate stack. Further work needs to be conducted to remove the TiO₂ residue left from TiN etching. Future efforts will either push to prevent the oxidation of TiN or for the targeted removal of TiO₂.

Acknowledgements:

I would like to thank my mentor and PI, Julian Gerharz and Dr. Jürgen Moers, for the time and resources they dedicated throughout my research experience. I also express appreciation for the helpful staff at the Forschungszentrum, and Prof. Dr. Detlev Grützmacher in particular. Lastly, I am grateful to Lynn Rathbun and Wolfgang Albrecht for their coordination of the iREU program.

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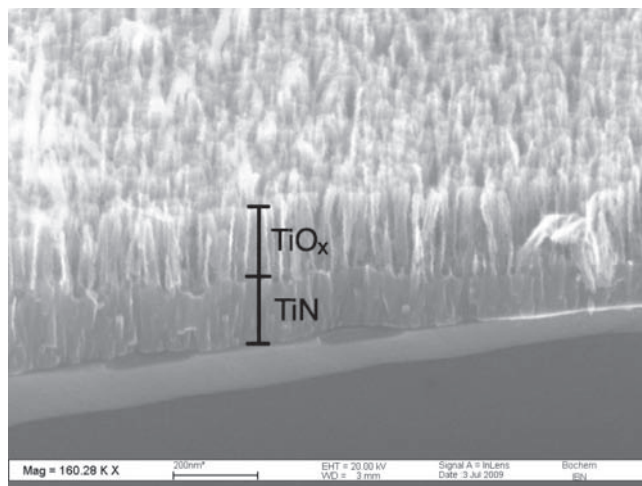


Figure 4: Titanium oxide residue after etching with Cl₂ plasma.