

Fabrication and Design of Nanowire Transistors

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Abstract and Introduction:

Modern society continues to crave smaller and energy saving electronics. For years, scientists have depended on the use of complementary metal-oxide semiconductor technology. However, with the year 2020 quickly approaching, devices are predicted to scale down to less than 45 nm in size, which exceeds the minimum dimensions of the current technology. Researchers have intensely labored to find solutions for this dilemma and one possible solution is III-V metal-oxide semiconductor field effect transistors (MOSFETs). These transistors specifically use nanowires as a bridge between electrodes. The wires are grown using elements from groups IIIA and VA of the periodic table, which together exhibit high mobilities making them more efficient for electron transport. The goal of this project was to fabricate and test a gallium nitride (GaN) MOSFET nanowire transistor.

Procedure:

To begin the process, we obtained a p-type silicon substrate which is a silicon wafer heavily doped with boron in order to decrease resistivity. Next, a silicon dioxide layer was grown on the silicon substrate to be used as the gate insulator for the device. The oxide layer was grown by the process called thermal oxidation to a required thickness of 50-100 nm. Thermal oxidation is defined as the formation of an oxide layer on the surface of a semiconductor. Before device oxidation, a series of trial runs was performed to calibrate the oxidation growth rate. The thickness of these layers was then measured by ellipsometry and 700 nm was determined best for the fabrication of this device.

An ohmic contact was formed on the backside of the silicon substrate which operated as the gate of the transistor. An ohmic contact is a metal-semiconductor junction allowing carriers to flow in and out of the semiconductor [1]. In order to form the contact, 100 nm of silicon-aluminum eutectic solution was thermally evaporated onto the backside of the substrate. Under high vacuum, the solution condensed and evaporated onto the back of our silicon substrate as a current was applied to the crucible—in turn heating up the source material. The substrate was then annealed at 500°C for 1 minute in order to reduce any barriers at the interface.

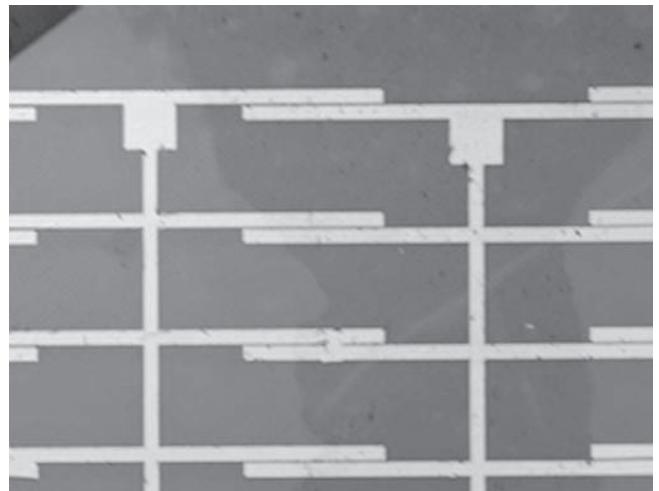


Figure 1: Mask #2 using photolithography, with source-drain metal contact fingers.

Photolithography was used to pattern the top surface for metal deposition of the source and drain contacts. The first mask used comprised of an array of $100\ \mu\text{m} \times 100\ \mu\text{m}$ squares, which were double-exposed to create the source and drain and to manipulate the distance between them. The average length of a nanowire was about $50\ \mu\text{m}$, so it was ideal to have distances less than $50\ \mu\text{m}$. This mask did not work so well because the nanowires seemed to land in open areas instead of across the source and drain. A second mask that had fingers branching off from the center was employed to increase the probability of landing a nanowire across the source and drain pads. This mask was also doubly-exposed to manipulate the distance between the source and drain fingers. This design proved to be much better as more nanowires landed across the source and drain pads (Figure 1). After photolithography, gold contacts were thermally evaporated onto the patterns. About 10 nm of chrome was evaporated onto our substrate as a primer and 100 nm of gold was evaporated as our metal contacts.

Lastly, we used a microgripper with a very fine tip and carefully collected gallium nitride nanowires from a gallium nitride sample. The nanowires attached to the tip by means of Van der Waals dipole-dipole attraction. After attaching

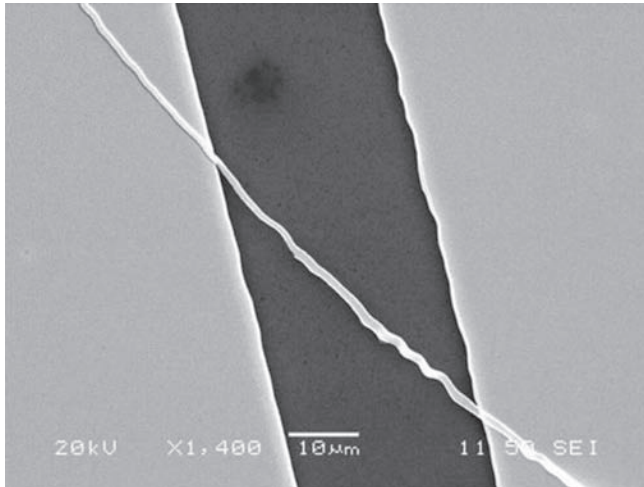


Figure 2: SEM micrograph of a nanowire transistor.

the nanowires, we carefully placed our substrate underneath the tip, avoiding vibrations, and applied methanol to the tip using a syringe. The methanol forced the nanowires off the tip and dispersed them onto the surface of the substrate.

Next, we used an optical and scanning electron microscope to view our samples and determined whether or not a nanowire was successfully deposited between two electrodes to complete the transistor. (Figure 2.)

Results and Conclusion:

After conducting current-voltage testing on these devices, it was concluded that the nanowires did not make full contact across the source and drain. We tested other devices and found operating devices when two test probes were applied (Figure 3). One probe was applied to one gold contact as the source and the second gold contact as the drain, which resulted in a linear graph. Lastly, we tested our annealed sample that was heated at 500°C for 1 minute.

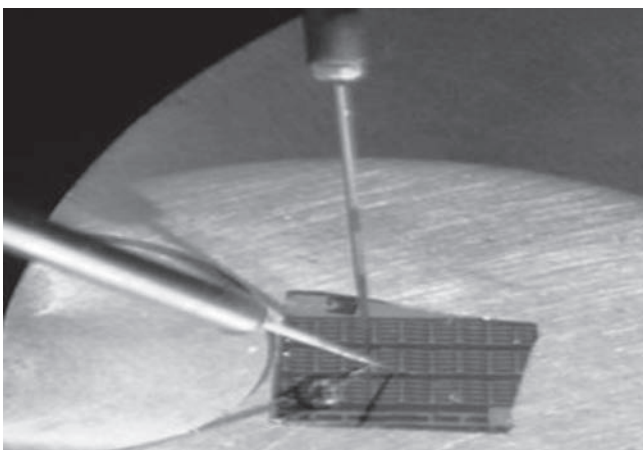


Figure 3: Nanowire transistor under test using probes.

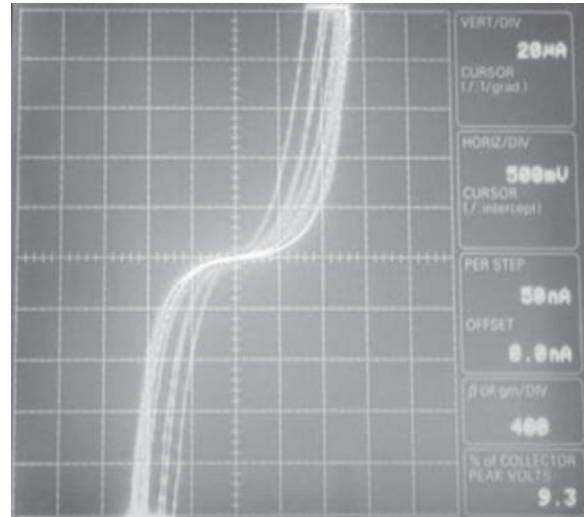


Figure 4: Current-voltage (I-V) curve of nanowire device.

As we tested this final sample, a third probe was applied to the back gate of the device. This was done by touching the probe onto the metal stage, which was in contact with the backside of the substrate [2]. This resulted in a back-to-back diode current-voltage curve of this device (Figure 4). The figure also shows the effect of point probe contacts via the noisy I-V current.

Future Work:

Since it was sometimes difficult to land nanowires across the electrodes, the ability to move them around on the surface using a micro-tipped cantilever would be immensely helpful. A second option would be to use e-beam lithography to pattern the samples after the nanowires were deposited. This technique would allow for the precise placement of the source and drain over the nanowires.

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- [1] Ohmic Contact Technologies. 2004. 14 July 2009. <http://www.SiliconFarEast.com>.
- [2] Wenzel, R.; Fischer, G.G.; Schmid-Fetzer, R. "Ohmic contacts on p-GaN (Part I): Investigation of different contact metals and their thermal treatment." 2001. 28 July 2009. <http://www.sciencedirect.com/>.