# Integration of Gallium Nitride Nanowires with Silicon Circuits

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## Abstract:

**Gallium nitride (GaN) nanowires synthesized previously through catalyst-free molecular beam epitaxy [1] were integrated with silicon circuits containing p-type metal-oxide-semiconductor field-effect transistors (MOSFETs). Basic silicon circuits were designed and fabricated, containing specific contact areas where nanowires could be deposited. GaN nanowires were aligned to the contacts by dielectrophoresis and contacted with an additional metal layer. Optical and scanning electron microscope (SEM) images and current-voltage measurements were taken to image and test the devices.**

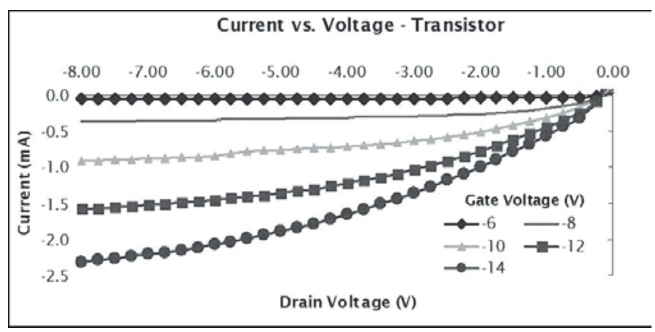
## Introduction:

GaN and its alloys with aluminum and indium have many potential applications due to the large range of their semiconductor band gap from the ultraviolet to infrared areas of the electromagnetic spectrum. Currently macroscale GaN is used in light emitting diodes and lasers found in cell phones, traffic lights, and DVD players [2]. GaN grown on the nanoscale as nanowires has benefits over its macroscale counterpart. Nanowires can be grown with a much lower defect density than macroscale GaN due to their small cross sectional area which avoids crystal lattice structure mismatch. GaN nanowires can also be grown directly on silicon substrates, commonly used in the electronics industry. Due to their high purity and convenient band gap, GaN nanowires have potential applications in quantum computing, biological sensing, and spectroscopy.

For any of these applications to become a real, marketable product, GaN nanowires must be integrated into circuitry. In this project, GaN nanowires were applied to integrated silicon circuits containing transistors and studied by current-voltage measurements and microscopy.

## Experimental:

A basic device was designed for the nanofabrication of the circuits to contain a p-type MOSFET connected to an area for nanowire applicationa. Devices were fabricated on <100> n-type silicon wafers. A layer of silicon dioxide was formed through wet oxidation with an automatic ellipsometer measured thickness of 0.713 ± 0.036 $\mu$m. Field oxide areas were etched in the oxide using negative resist photolithography (Futurrex NR9-1000PY, 1000 nm) and buffered oxide etch (JTBaker, 6:1). Boron was diffused into the field oxide regions using solid source boron nitride wafers (PDS) to form source and drain regions. Regions for gate oxidation were etched and oxidation took place in a dry/wet/dry oxidation sequence for a total oxide thickness of 0.1061 ± 0.0005 $\mu$m. The oxide was annealed at 910°C in a nitrogen environment. Via holes were etched over the source and drain regions. A thickness of 0.300 ± 0.003 $\mu$m of aluminum (Alfa Aesar, 100%) was thermally evaporated on the wafers and etched using a positive resist photolithography (Clariant



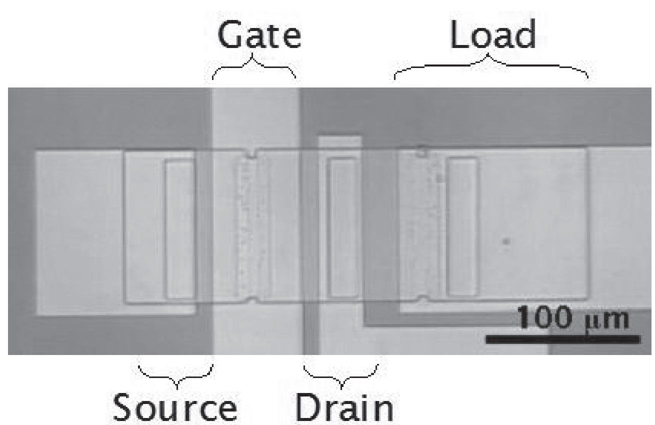




*Figure 1, top: Typical current-voltage curve for a transistor.*

*Figure 2, bottom: Optical microscope image of transistor with regions of the transistor labeled.*

AZ4210) and aluminum etch at 40°C (Transene type A) to form areas for nanowire application and complete transistor fabrication.

GaN nanowires were synthesized by catalyst-free molecular beam epitaxy according to previous reports [1]. The n-type doping variation as a fraction of total length of the nanowires was 30/50/20% high/undoped/high. Using a micropipette, 3.5 $\mu$L of a suspension of the nanowires in isopropanol were applied and aligned by dielectrophoresis [3]. Metal to contact the nanowires to the devices was formed through negative resist liftoff photolithography (Futurrex NR7-1500PY) and electron beam evaporation of 20 nm of titanium and 200 nm of aluminum. The metal was annealed by rapid thermal anneal at 500°C for 60 seconds in a 5/95% hydrogen/argon environment.

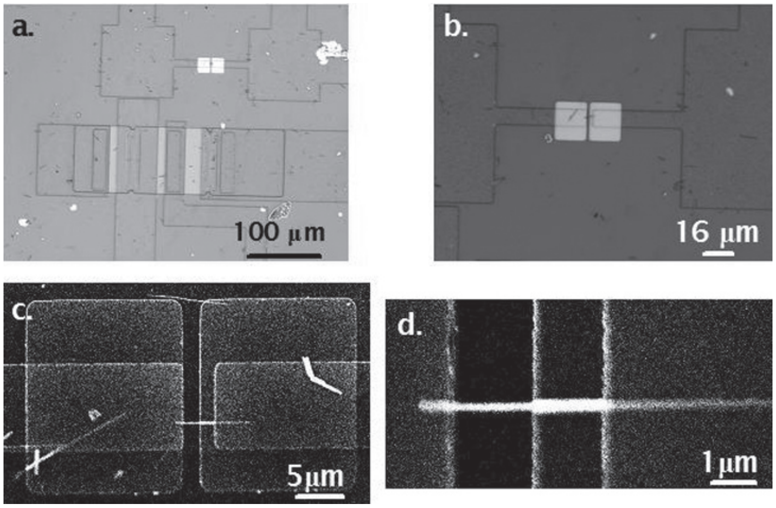



*Figure 3: Optical (a, b) and SEM (c, d) images of a final device.*

## Results and Discussion:

After fabrication, current-voltage measurements were taken of the transistors. Of the devices fabricated, 85% of the transistors were working. Typical current-voltage curves for a transistor can be seen in Figure 1. An optical microscope image of a transistor is shown in Figure 2.

After nanowire application, 27% of the devices had nanowires across the metal leads designed for the application and 8% had a single nanowire. Optical and SEM images were taken of the devices (Figure 3).

Current-voltage measurements were taken across the single nanowires. The measurements are indicative of Schottky-like or insulating behavior (Figure 4) which does not agree with previous electrical characterizations of the wires on simpler substrates. A possible explanation for this discrepancy could be the metal contacts landed on the undoped regions of the wire, causing a non-ohmic contact. The metal contact process could be adjusted so better contact could be made.

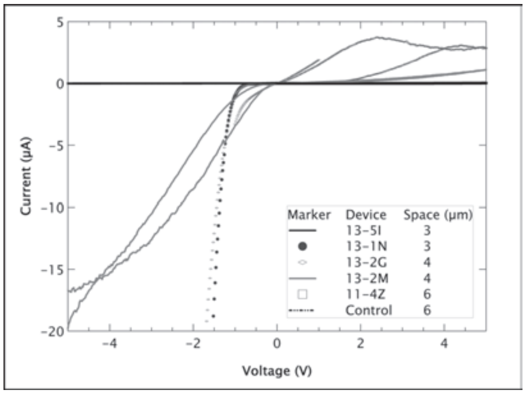



*Figure 4: Current-voltage measurements on single nanowire devices.*

## Conclusions:

In this project, a basic device was designed for a circuit containing a transistor and an area for GaN nanowires to be applied. Transistors were fabricated with 85% of the transistors working. GaN nanowires were applied to the devices using dielectrophoresis, and shown to work with an insulator or diode behavior.

Previous research has shown GaN nanowires have a good photoconductive response and a high potential as an ultraviolet photoconductor [4]. Completely depleted wires are insulating when measurements are taken in the dark, but in light, photons are absorbed by the wire, reducing the depletion region so the wire becomes more conductive. With the circuits fabricated in this project which contain depleted nanowires, future studies will demonstrate their application as an ultraviolet photoconductor. The transistors will also be studied to see if they amplify the photoconductive signal of the nanowires.

This is one basic step in the application of GaN nanowires with silicon circuits. Future work can expand by applying GaN nanowires to more complex circuitry and studying many of the possible applications of GaN in silicon circuits.

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