Sidewall Process for III-V MOSFET Fabrication

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Abstract:

Downsizing scalable transistor technology to increasingly smaller dimensions is necessary for more powerful electronics, as well as cheaper, more energy efficient devices, but *scaling* introduces new difficulties. While silicon technology may be reaching its limits, new materials, such as III-V semiconductor, are being developed for use in complementary metal-oxide semiconductor (CMOS) transistors with gates smaller than 15 nm. However, as gate lengths decrease, other features need to scale as well. Sidewalls, also called spacers, insulate the drain and source metal contacts from the gate of the transistor. Two techniques were investigated for producing thin, reliable sidewalls for use in metal-oxide semiconductor field effect transistors (MOSFETs).

Introduction:

As transistors continue to shrink, III-V semiconductor has a number of advantages over silicon. As a compound semiconductor, lattice spacing can be adjusted to allow very thin heterojunctions, and therefore, charge carriers may be closely confined in the channel, and offset the effects of scaling. Furthermore, with less affinity for oxygen, interfacial layers and native oxide formation are less of a problem. This material also has a lower electron effective mass, which should allow a higher drive current than in silicon transistors.

Metal-oxide semiconductor field effect transistors (MOSFETs) are widely used in digital and analog applications. Current between the source and drain is controlled by the gate voltage, which is electrically isolated by a thin insulating layer and sidewalls. Sidewalls, then, must support a large electric field without allowing large current leakage. They must also be as thin as possible, so that the gate has good control of the channel and can reduce the effect of interface traps on carrier population. In this project, over-etching of 30 nm sidewalls and slow deposition of thinner sidewalls were compared. The sidewalls of varying thickness were then electrically tested for their effectiveness as insulators.

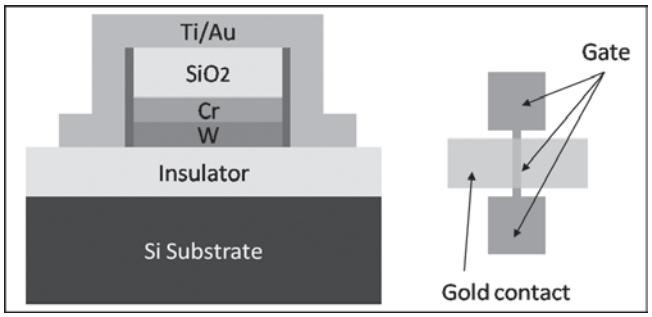

Figure 1: Structure used to test sidewall processes. Leakage current was measured by applying a voltage between the gold contact and the chromium of the gate.

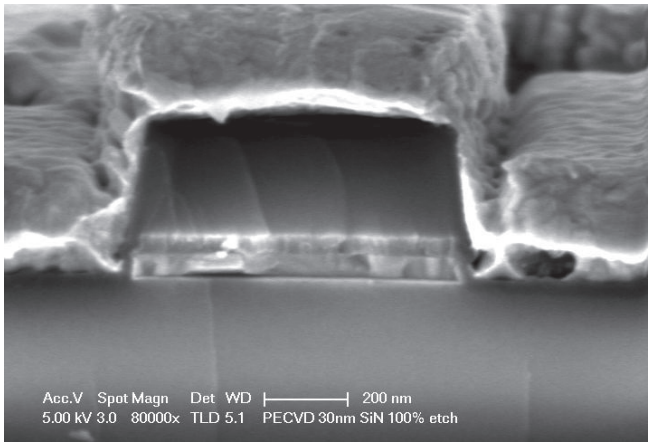

Figure 2: SEM of test structure. The sidewalls appear fairly thin, ~ 30 nm, and conformal to the gate metals.

Procedure:

To test the sidewalls, a gate stack similar to that intended for the full MOSFET was used; on silicon wafers, with a layer of either silicon dioxide or aluminum nitride, 50 nm of tungsten, 50 nm chromium, 150 nm of silicon dioxide, and another 50 nm of chromium as a hard mask. After depositing the gate stack, several etches are used to form the gate structure. SiN was then deposited in a thin film, and the horizontal regions were etched away with a low power anisotropic etch. Finally, gold contacts were sputtered on to allow close contact with the sidewall, and the gate contacts were exposed.

Results and Future Work:

The electrical properties of the sidewalls were measured by sweeping voltage across the gate and gold sidewall contacts. As expected, increased etching decreased the effectiveness and reliability of the sidewalls. Using plasma enhanced chemical vapor deposition produced conformal 30 nm sidewalls. However, over-etching on silicon dioxide did not result in significantly thinner sidewalls, as the reactants etched the field. Very slow deposition also formed thin, conformal sidewalls, although this technique was not been fully tested.

Very thin sidewalls can be made insulating on III-V semiconductor MOSFETs. This is encouraging for the development of these devices. Thinner sidewalls allow the gate to have greater control over the channel, and help increase the charge carrier concentration. Further experiments are needed to compare over-etching with slower deposition, using AlN instead of SiO_2. Because of the different chemical compositions of these insulators, over-etching should result in thinner sidewalls, while slower deposition may allow thinner sidewalls in the first place. The larger project is to make useful, small, high frequency MOSFETs out of III-V semiconductor. With gate lengths less than 15 nm, these materials should provide faster switching time, higher drive current and better drive control than other technologies.

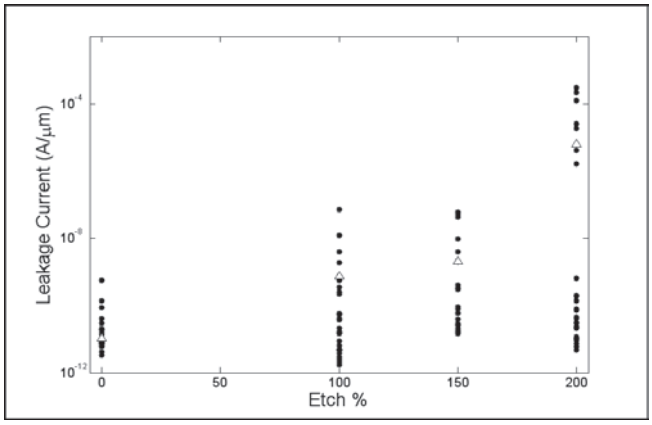

Figure 3: Plot of leakage currents for different etch amounts.

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