Transport Properties of InAs Nanowires for Applications in Quantum Information Processing

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Introduction:

Due to their high electron mobility, indium arsenide nanowires (InAs NWs) show promise for high-performance transistors and nanoelectronics. However, their transport properties are still not fully understood. The electron mobility of individual InAs NWs have been reported to be much lower than in bulk, suggesting strong electron scattering from the surface or from ionized impurities. Thus, protecting the surface may enhance transport properties.

In this work, NW transistors were fabricated using <110> InAs NWs. Room temperature measurements of top / back gate control and IV characteristics were performed and analyzed. Furthermore, the formation of quantum dots in InAs was investigated at low temperature.

Fabrication:

Undoped InAs NWs grown through metal organic vapor phase epitaxy (MOVPE) in the <110> crystal direction were dispersed on 25 fields of a degenerately n-doped silicon (Si) substrate, with a 100 nm layer of silicon nitride (SiN) above to act as a back gate. Scanning electron microscope (SEM) images of each field were taken and imported into AutoCAD to design ohmic contacts for selected NWs. Four single-strand isolated NWs were selected in each field—long, thin NWs were preferred. The chosen NWs had an average length of 2.3 μm and an average diameter of 140 nm. Where possible, four ohmic contacts were designed for each NW: the outer contacts were used as current source and drain, while the inner contacts were used to measure the voltage drop, avoiding effects of contact resistance.

Next, EBL and metal evaporation were performed to write the ohmic contacts. A 40 second Ar^+ ion etch was used to remove any native oxide that had formed on the NWs.

Next, a 50 nm layer of high-κ dielectric lanthanum aluminate ($LaLuO_3$) was spun onto the chip. A wet etch was performed to remove the dielectric above the contact pads, allowing direct ohmic contact with the NWs. Then, top gates were designed on AutoCAD for selected devices. Again, electron beam lithography and metallization were performed to write the top gates. After processing, the top gates were typically measured to be 170 nm wide and 110 nm apart. Finally, the chip was diced into 25 fields. Each chip was mounted onto a chip carrier and wire-bonded for low-temperature measurements in the cryostat.

A second set of NWs was prepared with the same processing, using thinner NWs (typical diameter of 40 nm). However, due to time constraints, only ohmic contacts were written for these devices.

Measurements and Analysis:

After writing ohmic contacts, the four-probe and two-probe resistances of the NWs were measured at room temperature. The contact resistances were found to be negligible in comparison to the resistance of the NWs. Next, the back gate control was measured in order to calculate the threshold voltages and transconductances of each NW. The length and diameter of each wire was verified using SEM pictures.

The back gate capacitance is seen in Equation 1, where L_{SD} is the wire length between the ohmic contacts, t_{ox} is the thickness of the substrate oxide (back gate), and d_{NW} is the diameter of the NW. The three-dimensional and two-dimensional electron concentrations are shown in Equation 2 and 3, respectively, where V_{TH} is the threshold voltage. Finally, the field effect mobilities were calculated using Equation 4, where g_m is the transconductance and V_{SD} is the source-drain voltage for which this value was measured.

$$C_{BG} = \frac{2\pi\epsilon_0\epsilon L_{SD}}{ln\left[\left(2t_{ox}+d_{NW}+2\sqrt{t_{ox}^2+t_{ox}d_{NW}}\right)/d_{NW}\right]} \quad \text{Equation 1}$$

$$n_{3D} = \frac{C_{BG}V_{TH}}{eL_{SD}\pi(d_{NW}/2)^2} \quad \text{Equation 2}$$

$$n_{2D} = \frac{n_{3D}d_{NW}}{4} \quad \text{Equation 3}$$

$$\mu_{FE} = \frac{g_m L_{SD}^2}{C_{BG}V_{SD}} \quad \text{Equation 4}$$

After the dielectric was deposited and the top gates were written, these values were measured again. Analogous formulae were used for calculating the top gate capacitance and resulting parameters.

The two-probe resistance of the NWs averaged 1.3 MΩ before the deposition of the dielectric, but was reduced to an average of 0.29 MΩ afterwards (see Figure 2). Consequently, the threshold voltages were also found to be lower, resulting in increased electron concentration and increased field effect mobility in the wires (see Figure 3). This suggests that the presence of the dielectric enhances strong surface transport states and that the transport in the NWs resembles that of a two-dimensional electron gas (2-DEG). Moreover, no correlation was found between wire geometry, typically parameterized by length divided by cross-sectional area, and wire resistance. This suggests that the wire's complex crystal structure, which alternates randomly between wurtzite and zincblende, plays a stronger role in determining the resistance of the NWs than the geometry itself.

Next, the device with the best top gate control was selected for low-temperature measurements. The hysteresis of the top gates was verified to be low, and the two most symmetric and adjacent top gates were chosen for quantum dot measurements at approximately 2 Kelvin.

Applying a gate voltage on adjacent top gates formed a double energy barrier, between which quantum confinement of electrons was realized. By fixing the gate bias on one top gate and sweeping the other, the energy barrier was dynamically modified. Current through the wire (electrons escaping the quantum dot) was then measured as Coulomb peaks (see Figure 4). These measurements prove the successful formation of a quantum dot in InAs NWs.

Conclusions:

The transport properties of InAs NWs were investigated at both room and low temperatures. The deposition of high-κ dielectric was found to induce strong surface states, enhancing electron mobility. Furthermore, the a quantum dot was successfully formed in InAs.

Future Study:

There was no correlation found between wire geometry and wire resistance, suggesting the need to further study the crystal structure of these wires using TEM analysis. Additionally, measurements on the second prepared sample will yield more information on the quantum confinement regime (diameter < 80 nm).

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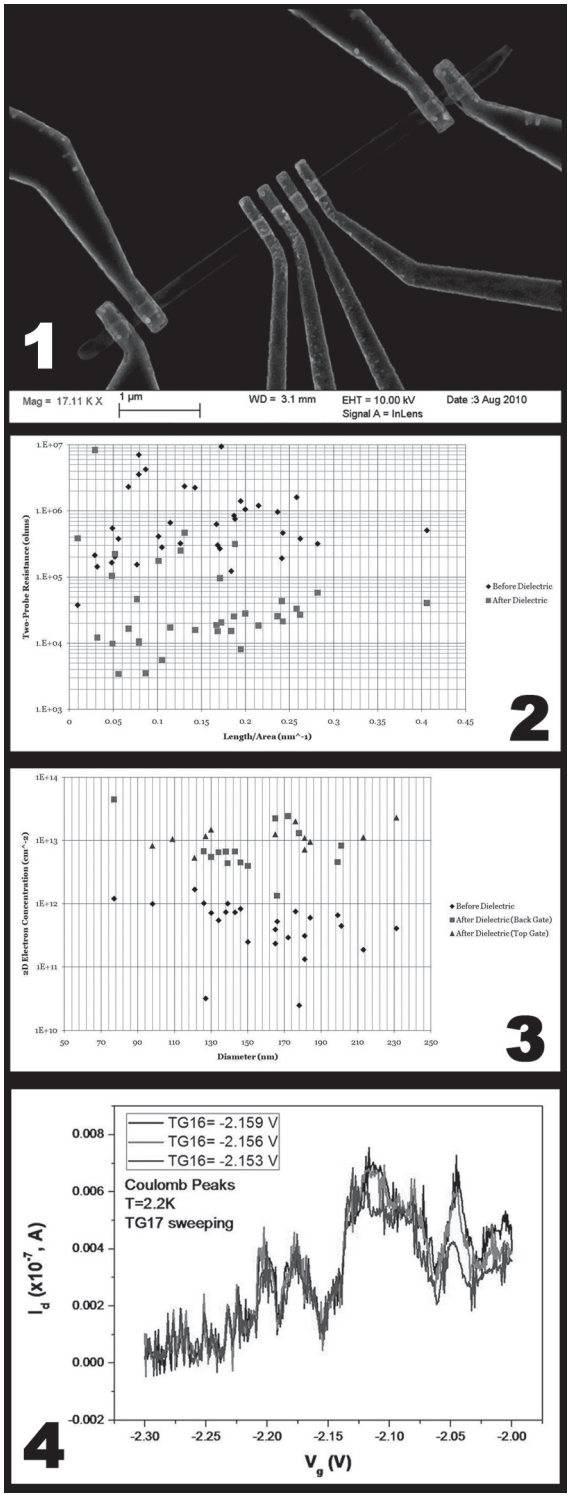

Figure 1, top: SEM of a typical NW transistor is shown with four ohmic contacts and four top gates.

Figure 2, upper middle: The 2-probe resistances of the NWs before (◆) and after (■) the deposition of the dielectric are compared.

Figure 3, lower middle: The 2D electron concentration in the NWs is calculated before dep. of the dielectric using the back gates (◆), and after dep. using both the back gates (■) and the top gates (▲).

Figure 4, bottom: One top gate voltage is held fixed while the other is swept. Coulomb peaks (nonzero current) can be observed at specific values of gate bias.