Using Electron Beam Lithography for Nanowire Transistor Fabrication

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Abstract:

The objective of this project was to fabricate a nanowire transistor using electron beam (e-beam) lithography. Nanowire transistors are devices made to solve the scaling problem that contemporary silicon transistors have begun to face. By placing nanowires on the surface of silicon chips, as opposed to using conventional photolithographic processes to create gates, the gate length restriction imposed on conventional methods can be overcome. To start this process, a 60-100 nm silicon dioxide (SiO_2) layer was grown by dry thermal oxidation on a boron-doped, 0.005 Ω-cm resistivity, <100> silicon wafer. A 10 nm layer of chrome (Cr) and a 100 nm layer of gold (Au) were then evaporated onto the backside of the Si wafer and tested for ohmic behavior. Photolithography was then performed to create Cr/Au (10nm/100nm) fingers and pads on the top oxide layer. Nanowires were then deposited on the top surface by brushing with cloth followed by e-beam resist deposition. Scanning electron microscopy (SEM) was performed to locate the nanowires relative to the fingers, and holes were developed in the resist and coated with Cr/Au (10nm/20nm) to attach the nanowires to the fingers. Devices were then tested.

Introduction:

Since the second half of the twentieth century, transistor technology has been the driving force behind the evolution of modern electronic systems. There are semiconductor devices that function as on/off switches or amplifiers in logic circuits. As such, the more transistors you can fit on a chip, the greater computational power you can achieve. Therefore, modern electronics are dependent on the steady miniaturization of transistors. Currently, the predominant transistor fabrication method is the complimentary metal oxide field effect transistor (CMOSFET). However, the CMOSFET method is reaching its limits in reducing the size of transistors.

Within the last few years, the National Institute of Standards and Technology (NIST) proposed a nanowire transistor design to overcome the restrictions conventional photolithographic methods place on device scale. Additionally, NIST claimed that nanowire transistors reduce current leakage, switch more effectively, and would allow industry to continue utilizing its silicon infrastructure. For this project, a manual stage scanning electron microscope and electron beam writing setup was used specifically to test whether nanowire transistors could easily be fabricated.

Experimental Procedure:

To start the process, a 60-100 nm layer of SiO_2 was grown on a low resistivity *p*-type <100> silicon wafer. The backside oxide layer was subsequently removed with hydrofluoric acid. A layer of Cr/Au (10nm/100nm) was then deposited onto the backside by e-beam evaporation in order to create the backgate contact. This metal-semiconductor contact was then tested for ohmic behavior. The current-voltage behavior of the contact is shown in Figure 1.

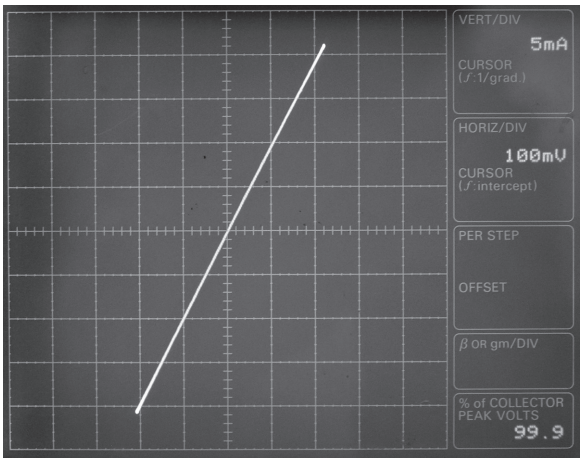

Figure 1: IV characteristics of backgate contact. Exhibits ohmic characteristics

Next, Microposit S1818 resist was spun on the topside and exposed through a mask to form fingers and pads. A layer of Cr/Au (10nm/100nm) was evaporated onto the sample and the excess metal was lifted off to create metalized fingers and pads on the oxide surface, which served as transistor sources and drains.

In order to place the nanowires in close proximity to the fingers, a KIMTECH wipe was gently brushed over a sample of gallium nitride (GaN) nanowires (approximately 200 nm in diameter) and then brushed onto the sample. MicroChem 950PMMA resist was then deposited onto the sample and loaded in the SEM. Once the nanowires were located, patterns were written into the resist using Raith Elphy e-beam writing software to connect the nanowires to the source and drain fingers. This part of the work was critical because the e-beam used for imaging (not etching) also partially exposed the sample. Much effort was undertaken to optimize imaging conditions to avoid unwanted pre-exposure of the resist. Optimization parameters included accelerator voltage, spot size and contrast. After e-beam writing, the samples were developed using a 1:3 mixture of methyl isobutyl ketone and isopropanol. A layer of Cr/Au (10nm/20nm) was evaporated onto the sample and lifted off. An image of the completed device is shown in Figure 2.

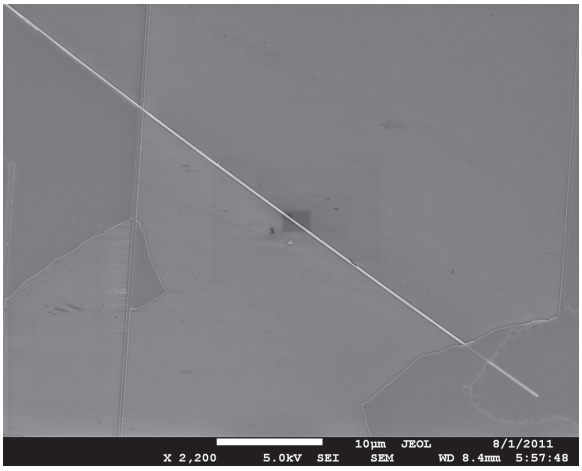

Figure 2: Nanowires connected to source and drain contacts with Au. Represents completed device.

Results and Conclusions:

Near-ohmic contacts were established between the source/drain contacts and the gallium nitride nanowires; see Figure 3. Unfortunately, when the gate-to-source bias was adjusted between -20V and +20V, no change was observe in the voltage-current curve for the transistor; see Figure 4. It is speculated that the GaN nanowires were heavily doped and therefore higher bias voltages were needed to modulate the current across the device.

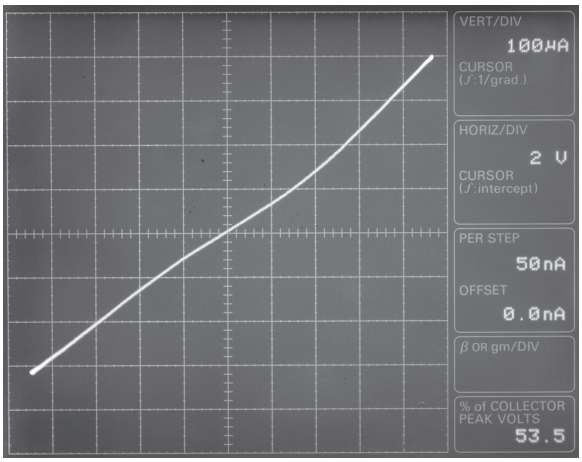

Figure 3: IV characteristics of topside contact (source to drain). Exhibits near-ohmic characteristics.

In conclusion, SiO_2 was grown at desired thickness on wafer. Ohmic and near-ohmic contacts were established on the device. Nanowires were found and connected to pads with SEM and electron beam lithography.

Nanowires conducted current, however, bias modulation did not exhibit proper transistor characteristics.

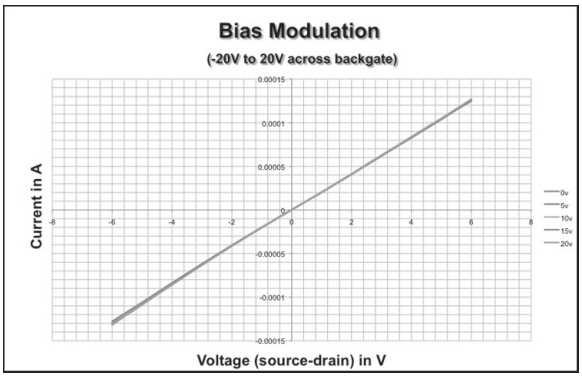

Figure 4: Bias modulation of device from -20V to 20V. Characteristics change in slope does not occur as with usual transistors.

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References:

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