Fabrication of Free-Standing Graphene Films for Probing the Ultrafast Electron Dynamics

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Introduction:

Graphene has generated much interest due in part to very high carrier mobility (200,000 $cm^2V^{-1}s^{-1}$) and ultrafast carrier relaxation time (<100fs) [1, 2]. However, trapped charges in the substrate or at the substrate/graphene interface couple with the graphene, causing doping effects and lowering the carrier mobility [1, 3]. In order to accurately study the ultrafast electron dynamics in graphene, these negative substrate effects must be mitigated. Therefore, this project aims to fabricate free-standing graphene grown by chemical vapor deposition (CVD).

The substrates for free-standing graphene were fabricated from silicon wafers by etching holes (2-50 μm) with potassium hydroxide (KOH). CVD graphene with domain sizes from 20-50 μm was grown and transferred to the patterned silicon wafer. High-quality, free-standing graphene with low *p*-doping was observed and confirmed with Raman spectroscopy.

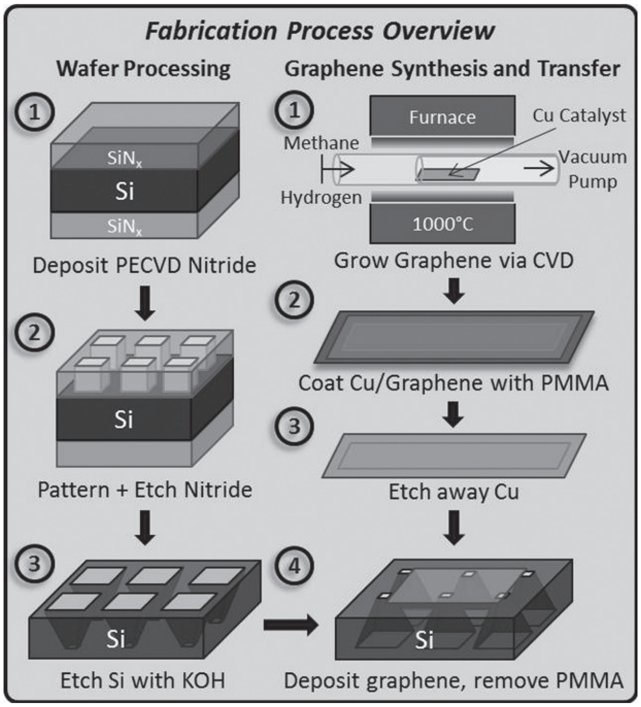

Figure 1: Illustration of the wafer processing and graphene growth and transfer methods used to fabricate free-standing graphene.

Procedure:

Fabrication of free-standing graphene was accomplished in two distinct processes (see Figure 1). In the first process, holes were etched into double-side polished 100 μm thick 2-inch <100> silicon wafers. Low-stress silicon nitride was deposited via plasma enhanced CVD to create a ~ 330 nm layer to serve as a mask for etching. Negative photoresist was applied to both sides of the wafers and holes were patterned and etched into the nitride on the back side with a buffered oxide etch. A 250-minute KOH etch (which etches the <100>-plane ~ 100 times faster than the <111>-plane) at 70°C was then used to create holes through the wafer, 2-50 μm wide on the front side.

In the second process, graphene was grown via CVD on a 25 μm copper foil catalyst [4]. More than 90% of this graphene was single layer since graphene can only grow where the copper catalyst is exposed. The CVD growth process was conducted in a 10 mTorr vacuum at 1000°C for four hours while methane (0.2 sccm) and hydrogen (10 sccm) were injected into the system. Ultra-low-pressure growth was chosen to minimize the number of graphene nucleation sites on the catalyst and to allow for each domain to grow to its maximum size. Following growth, the graphene was transferred to the patterned silicon wafer [5]. For this process, the copper was spin-coated with a layer of poly(methyl methacrylate) (PMMA) following graphene growth. After allowing the PMMA to cure, a 0.5M ferric chloride hexahydrate solution was used to etch the copper and leave graphene stabilized with PMMA. The samples were rinsed with deionized water before being transferred to the silicon wafer. After drying, the PMMA was removed in a furnace (400°C, one hour) in an H_2/N_2 atmosphere.

Results:

The graphene was characterized via scanning electron microscopy (SEM). This analysis revealed single-crystal graphene domains ranging in width from 20-50 μm, with an average size of approximately 30 μm. Graphene was found to cover between 80% and 90% of the copper surface (see Figure 2). Large domain sizes (> 20 μm) and high coverage was needed to maximize the probability that a single-crystal graphene domain would cover a hole in the silicon wafer.

The finished samples were examined by optical microscope. The presence of small particles in the middle of a hole in both light and dark field modes (see Figure 3) was found to be a clear indicator that free-standing graphene was present.

Raman spectroscopy was used to verify the presence of single-layer graphene and determine its quality and doping. Figure 4 compares the Raman spectrum for a sample of free-standing graphene with a sample of graphene on silicon. The Raman spectrum clearly shows the characteristic G and 2D peaks of graphene. The insubstantial D peak in the spectrum of the suspended graphene indicates that it is largely defect free and that the hole is covered by a single-crystal graphene domain (domain edges contribute to the D peak). Analyzing peak shifts and the 2D/G peak ratio provides information about the doping characteristics of the sample. Both the G and the 2D peaks are down-shifted in comparison to the graphene on silicon with native oxide, indicating lower *p*-doping. The 2D/G peak ratio of 3.6 further indicates that this graphene is minimally doped and high-quality [6, 7]. Moreover, there is no PMMA signature in the Raman spectrum for the suspended graphene, indicating that the chosen removal method was effective.

Conclusions:

In conclusion, free-standing graphene was fabricated via CVD growth and transfer to etched silicon. CVD growth reliably produces high-quality single-layer graphene ideal for this study. Graphene was identified by optical microscope on 15 holes in four wafers and verified by Raman spectroscopy. High-quality free-standing graphene was observed over holes as large as ~ 20 μm. The *p*-doping level in the free-standing graphene was observed to be lower than in the graphene on silicon with native oxide. With the development of this free-standing graphene, further studies in fundamental physics are now possible.

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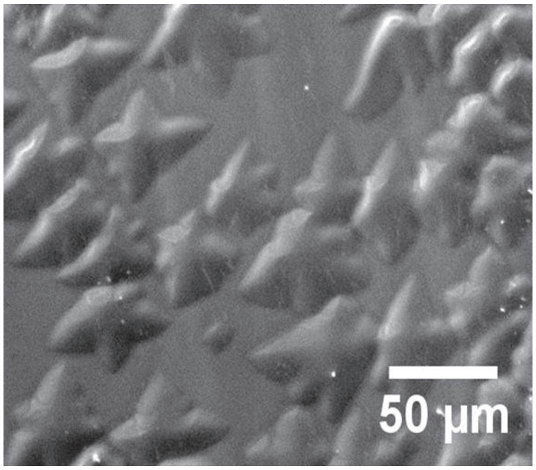

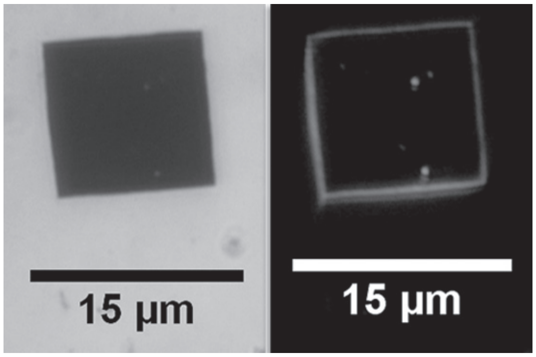

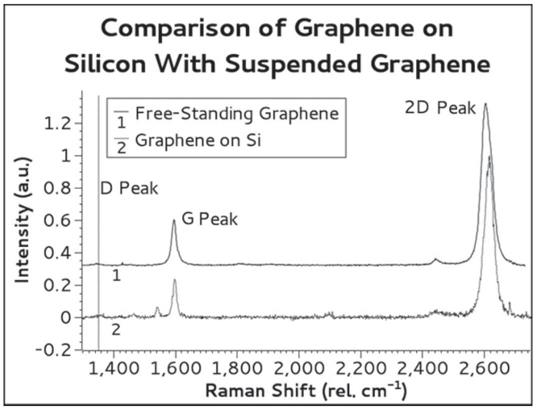

Figure 2, top: SEM image showing 20-50 µm graphene domains covering 80-90% of the copper.

Figure 3, middle: Light Field (left) and Dark Field (right) optical microscope images of free-standing graphene, as indicated by suspended particles.

Figure 4, bottom: Comparison of Raman spectra for graphene on silicon and free-standing graphene.