The Micro-Fabrication of a Composite Thermal Capacitor

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Abstract:

In order to maintain the rate of advancement achieved in traditional microprocessor technology over the past few decades, recent studies have focused on three dimensional stacked microprocessor architectures because of their potential computational advantages as well as a decrease in noise, power consumption, and reduction in parasitic capacitance. The implementation of this solution has been limited by the generation of transient hot-spots. To manage the thermal impact of these transient hot-spots, we fabricated composite thermal capacitors (CTC), which locally increase the thermal capacitance of the chips in the vicinity of the hotspots, allowing for longer device operating times. The fabricated and tested prototype devices consist of phase change materials (PCM), and heat spreader matrices monolithically integrated into silicon chips also containing micro-heaters, which simulate microprocessors. The CTC's novelty arises from its efficient combination of high thermal conductivity materials with PCMs to yield enhanced effective thermal conductivity while retaining desirable thermal capacitance in order to increase the micro-processor operating time. By using microfabrication techniques (Figure 1) such as chemical vapor deposition, photolithography, metal deposition via electron beam evaporation and sputtering, and reactive ion etching, we constructed a fabrication outline for a prototype CTC device, while a heater was monolithically fabricated with the CTC to simulate the microprocessor.

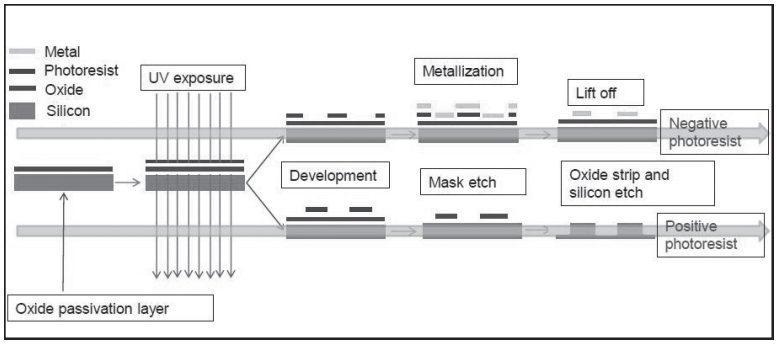

Figure 1: Fabrication outline for positive and negative photoresist.

Fabrication Outline:

An oxide passivation layer was deposited on the front and back side of a blank silicon wafer in order to control current flow through the heater coils and also to act as a mask for the CTC patterns. The heater was fabricated on the chosen front side.

Futurrex NR71 3000P positive photoresist was spun on the front side for the heater device lithography. It was essential to run a descum process after the lithography process in order to strip remnants of resist left on the pattern. Using a metal evaporator, 250 A of titanium (Ti, adhesion layer), and 2500 A platinum (Pt, resistive property) was deposited. After lift-off, the leads, which channel current to the heater device, were patterned using NR71 3000P photoresist.

For the lead metallization, 500 A of Ti, 3000 A copper (Cu, electrical properties), and 2000 A of gold (Au, wire bonding purposes) were deposited using a metal evaporator.

On the back side, Microposit 1827A positive photoresist was spun for the CTC lithography. In order to attain the monolithic integration of the heater with the CTC device, a back side alignment (BSA) procedure was used. After the lithography, the wafer was mounted CTC side up using SPR 220 7.0 photoresist, done to prep the wafer for reactive ion etching. A mask etch was done to remove the oxide on the CTC pattern. Since the surface of the patterns was now exposed, a 200-250 μm vertical depth trench etch of silicon was performed to produce the PCM trench, using

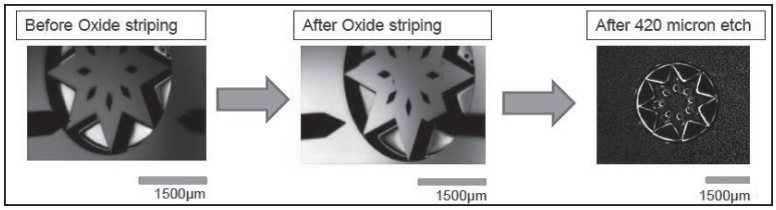

Figure 2: CTC etch process.

an inductively coupled plasma. In order to reduce the temperature gradient between PCM and the hotspot, the wafer was thinned by stripping the surface oxide, thus exposing the surface to the etching plasma (Figure 2); ideally the surface and trench etch rate should now be equal, therefore thinning the wafer. Once the change in distance from the PCM trench to the heater was between 75-100 μm, 500 A of Ti and 1.5 μm of Pt were added for wettability with the PCMs.

Fabrication Challenges:

For the heater fabrication, some issues regarding pattern adhesion arose after development due to an anisotropic post exposure bake. Since the patterns were not well baked, after development some features were detached from the device, thus leaving the device useless. By using a vacuum contact post bake, the wafer was brought closer to the hot plate, therefore increasing the level of uniformity and reducing the amount of device defects (Figure 3).

The etching equipment for the CTC device operates by cooling the backside of the wafer while the plasma is etching through the patterns to increase the etching quality. So the ideal adhesion material was thermal grease because of its high thermal conductivity. But since a low thermal conductive material (SPR 220) was used, the cooling was anisotropic, thus producing a low quality etch. Another issue that arose during the CTC etch was the trench depth decreased during the thinning step, meaning that the etch surface etch rate was not equal to the trench etch rate. In order to increase the directionality of the etching plasma, the etching pressure was reduced by 20%; as a result the etch rate was relatively equal, therefore maintaining a desirable trench depth.

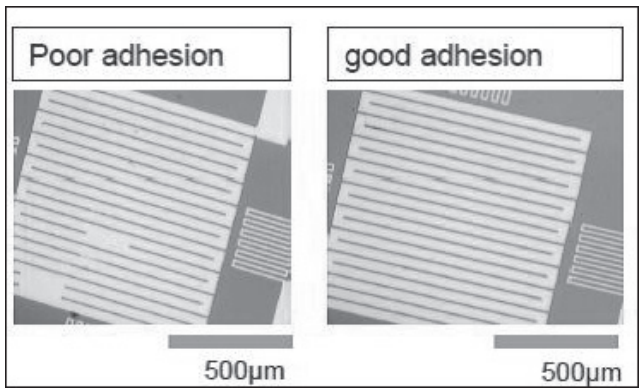

Figure 3: Before and after vacuum post bake.

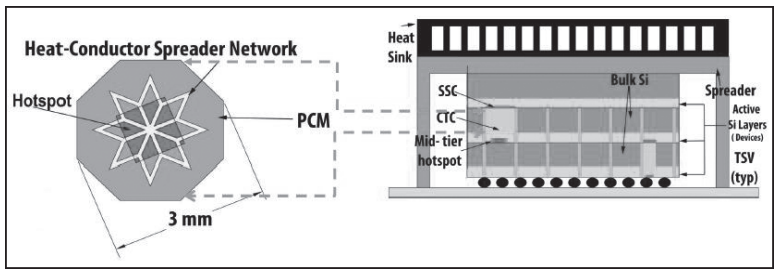

Figure 4: CTC SSC assembly.

Conclusion:

Using thermal grease as the adhesion material increased the difficulty of un-mounting the wafer after final CTC processing, which increased the chances of damaging the devices; so by using instead a thermal conductive material with adhesive properties similar to SPR 220, we will be able to increase the quality of the CTC device.

In conclusion, we were able to construct a fabrication outline for a CTC device which includes procedures that can be followed to reduce device defects.

Future Work:

Tin-, lead-, and indium-based alloys, like alloy 134 and 174, will be deposited into etched trenches to prep the CTC device for testing. The CTC device will be tested by being assembled in a microprocessor-like structure combined with a solid state cooler (SSC) (Figure 4). The goal of the SSC is to regenerate the phase change material during the idle state of the core in order to allow the PCM to absorb heat effectively during the active mode of the core.

Acknowledgements:

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References:

[1] Green, C.E., A. G. Fedorov, and Y.K. Joshi (2011); "Thermal Capacitance Matching in 3D Many-Core Architectures." In IEEE SEMI-THERM 27.