Characterization of Floating-Gate Graphene

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Abstract:

Graphene is known for its high electron mobility (over 5,000 $cm^2V^{-1}s^{-1}$). However, because of its zero bandgap, graphene is a non-ideal semiconductor for switches. Theoretical and experimental results indicate that graphene nanoribbon (GNR) opens up a bandgap because of the quantum confinement effect (inversely proportional to the width). Therefore, it is crucial to control the width of the growth down to sub-10 nm with a reliable method. However, the line edge roughness (LER) from electron beam (e-beam) lithography or photolithography degenerate the quantum confinement, which hinders the further application of GNR. Thus, combining the controllable width and sharp edge was one of our technical goals. The spacer lithography, a state of art patterning technology, has been widely used in current industry to create sub-pitch smooth patterns such as FinFET (a non-planar, double-gate field effect transistor). We combined e-beam lithography with well-calibrated spacer lithography to seek a better electrical performance on the metal-oxide semiconductor field-effect transistor (MOSFET) structure using graphene as a channel layer.

Calibration Procedure:

The calibration process to obtain the GNR needed for our transistor started with finding the optimal etching selectivity between silicon (Si), silicon dioxide (SiO_2) and silicon nitrate (Si_3N_4) for the spacers that would reduce the LER and scale the width down to 10 nm. We started with a 4-inch Si wafer and deposited 180 nm of SiO_2 to act as our spacer sidewalls, followed by a deposition of 20 nm of chrome (Cr) as to act our mask, obtain more anisotropic features, and avoid a facet. We then spun 3 μm of positive photoresist, exposed and developed vertical lines across the wafer, and followed by etching the Cr mask and removing the photoresist.

We etched the spacer sidewalls and used a scanning electron microscope (SEM) to check the sidewalls, as seen in Figure 1. After we found the right SiO_2 deposition and correct etching times and rates, we moved on to depositing the Si_3N_4. We found that the Si_3N_4 deposited and the spacer widths obtained were directly proportional. We started by depositing 50 nm of Si_3N_4 and obtained about 53 nm spacer sidewalls.

For our calibration process, we deposited down to 40 nm Si_3N_4 and obtained about 39 nm spacers. We checked with the SEM to assure that the spacers were smooth, and we also checked the thickness, as seen in Figure 2. After we had the right spacer sidewall as well as the spacers, the next part of our calibration was finding the right chemistry to etch the Si_3N_4.

We changed the power as well as the plasma density in the Oxford 100 etcher, because with higher power, we obtained better anisotropic

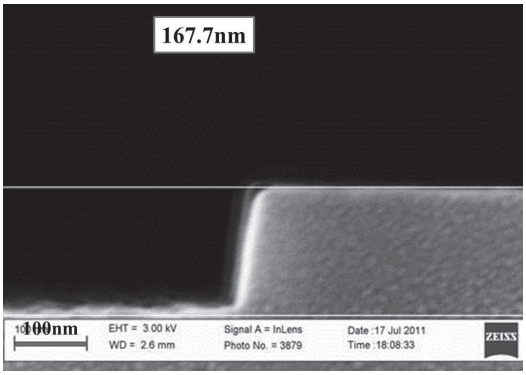
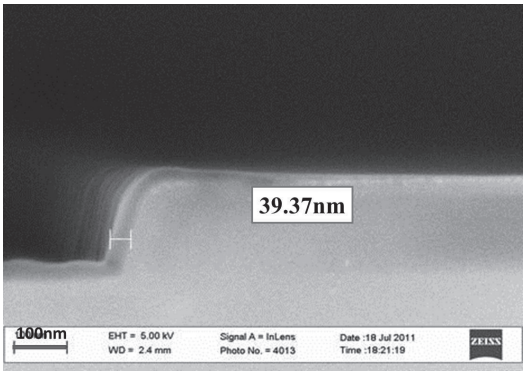


Figure 1, above: SEM of our sidewalls.

Figure 2, below: SEM of our spacers, checking for smoothness and thickness.



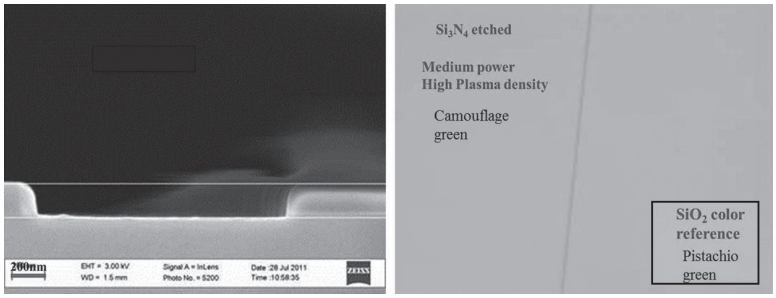


Figure 3: We used SEM and optical microscopy for color reference and final chemistry.

features, and with higher plasma density, we obtained a cleaner and smoother edge. Although we assumed that high plasma density and high power would give us our best etching result, we found that instead, it resulted in over-etching the Si_3N_4; but medium power and high plasma density did not.

By checking with the SEM and with optical microscopy for the color reference, we found our final chemistry as seen in Figure 3. With the right chemistry, and the right deposition times and rates, our calibration process was done. The selectivity we obtained was about 3:1, and although ideally we were looking for a higher selectivity, our resulting selectivity was acceptable.

Experimental Procedure:

To begin our experiment, we grew about 90 nm of SiO_2, which was for the graphene to reflect from our wafer. We carved a coordinate system to help us relocate the graphene. Using the "tape method," we exfoliated graphene and applied it on our wafer, being very careful not to apply too much pressure nor too little — to avoid dense graphite and too small graphene. The next steps were to use optical microscopy to locate graphene that was greater than 20 μm wide and record its location.

We then created a layout of lines that were 50 nm thick by 20-30 μm long, depending on the graphene thickness, and we send it to the e-beam tool to expose those lines across the possible graphene. But before this step, we had to protect our graphene and add spacer sidewalls.

We wanted to deposit a protection layer for the graphene, because since our wafers were going to be exposed to oxygen plasma, we didn't want the graphene to go away. We deposited the SiO_2 and the Cr mask using the deposition rates and times found in the calibration process, and then we wrote our layout with 200 nm of negative e-beam resist using e-beam lithography. We followed with another calibration process, and then finally deposited about 30 nm of Si_3N_4 to be sure to obtain spacers. Ideally we would have wanted 80 nm total, 20 nm spacers and 40 nm of SiO_2.

Results and Conclusion:

Unfortunately we were unable to finish this project, and so were not able to see what spacers we finally obtained, but we assume that we obtained about 100-110 nm total. Although we were unable to finish, we did obtain the graphene nanoribbon. The next step will be to write our source/drain with positive resist, then wet etch the SiO_2 and protection layer, and finally deposit 1 nm of Cr as an adhesive layer for the 100 nm gold. We'll use the lift-off method to remove excess metal as well as other excess material. Finally we'll clean the oxide off the back of our wafer and deposit 1 nm of Cr and 100 nm of Au as our back gate. Electrical measurements will be implemented to investigate the device characteristics.

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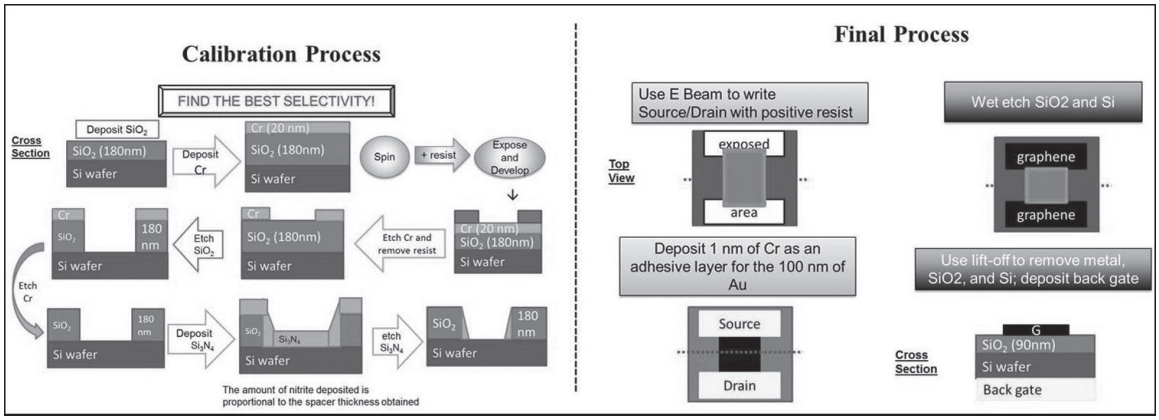

Figure 4: Here we see our calibration process flow as well as our future work process flow.