Devices for Investigating Electrical Transport in Topological Insulators

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Abstract:

Topological insulators are a recently discovered class of materials that have a unique set of properties. These materials are electronically insulating in the bulk, but have conducting states that exist only on their surface. Bismuth (III) telluride (Bi_2Te_3) and bismuth (III) selenide (Bi_2Se_3) are two examples of topological insulators that we investigated here. We attached leads to bismuth telluride nanostructures, grown by solvothermal synthesis, using aligned electron beam lithography. We also fabricated gated Hall bar structures from bismuth selenide thin films, which were grown using molecular beam epitaxy by collaborators.

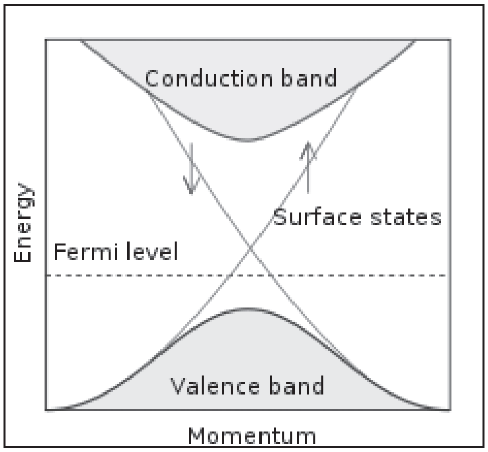

Figure 1: The spin of the carrier is locked to its momentum. The result is a strong protection of the carrier from back-scattering.

Introduction:

Topological insulators are a new class of materials that have unique properties. These materials are electronically insulating in the bulk, but have conducting states at the surface. This can better appreciated in Figure 1. The carriers have their spins locked perpendicular to their momentum. There are many examples of these materials, but only two were of our interest.

The first one was bismuth telluride (Bi_2Te_3), which was synthesized in the lab in the configuration of nanorods with the dimension of few micrometers long and several hundred nanometers wide. The other one was bismuth selenide (Bi_2Se_3), which was grown on a gallium arsenide substrate on top of zinc selenide with molecular beam epitaxy with a thickness of 10 nm and protected by a thin layer of selenium.

Our goal was to fabricate devices that could be use to measure electronic properties of these materials.

Experimental Procedure:

The fabrication process for the Bi_2Te_3 devices was divided in two steps. The first was the synthesis of the nanorods and the second was the fabrication itself. The nanorods were grown by solvothermal synthesis.

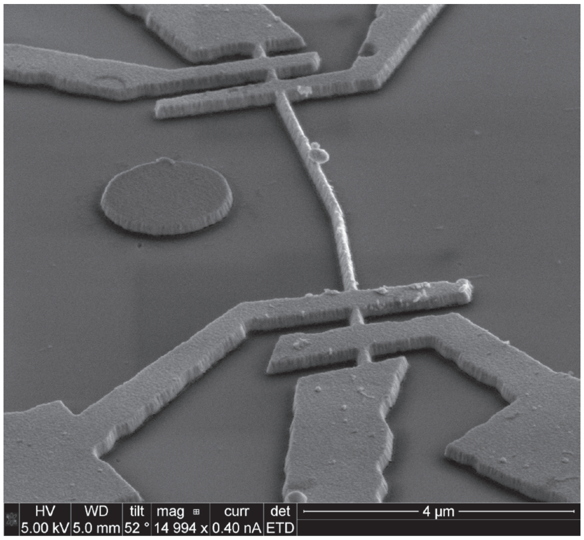

Figure 2: The nanorod is the long wire that is seen in the middle. The circular feature is a gold alignment mark. The source and drain are at the ends of the wire with the four leads in between.

In a vessel a suspension, composed of ethylene glycol, high purity polyvinylpyrrolidone (PVP), ethylenediamine tetraacetic acid (EDTA), tellurium and bismuth oxide, was mixed until the suspension was homogeneous. The vessel was sealed, heated up to 220°C, and sustained for at least four hours. The product was collected using a high speed centrifuge and washed with ethanol and water. This process was repeated until all the ethylene glycol was replaced. The now-clear suspension was cast onto a silicon wafer previously prepared with gold alignment marks. Resist was spun on top of the wafer and an electrode pattern, consisting of a gate, a source, a drain, and four additional contacts, was exposed using electron beam lithography. Following development of the resist, gold was evaporated onto the wafer surface and the resist layer was lifted off to leave the desired configuration of electrodes. An example of the device can be seen in Figure 2.

The process for fabricating a Hall bar structure on Bi_2Se_3 started by spinning, patterning and developing a photoresist layer. This resist protected the covered area of the Bi_2Se_3, while the rest of the surface was etched away down to the gallium arsenide substrate using an ion mill. After removal of the resist, the chip was heated to 220°C to evaporate the Se layer, exposing the Bi_2Se_3. Silicon nitride was then deposited on the entire chip to protect the Bi_2Se_3 surface and was spun with photoresist, patterned and developed once more. To make electrical contacts, silicon nitride was etched way at the desired locations and gold was deposited using a liftoff process. The device cross section is shown in Figure 3. The last step is to deposit larger gold leads to connect to the contacts. The final device can be seen in Figure 4.

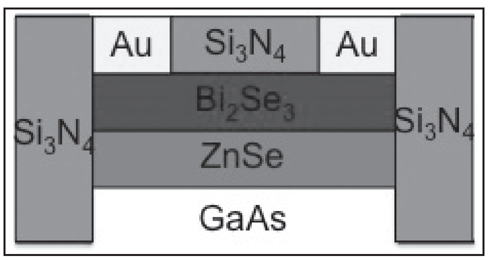

Figure 3: The different layers of the bismuth selenide chip. The gold leads are insulated from each other by the silicon nitride.

Figure 4: Microscope picture of a typical device geometry. Gold leads are in yellow (light gray) and silicon nitride is the light green (medium gray).

Results and Conclusions:

The Bi_2Te_3 synthesis proved to be difficult, but with a well establish method, it was possible to fabricate several devices from a single cast. Initially the selenium vaporization step caused trouble for the Bi_2Se_3 devices, but we solved this and made many of the Bi_2Se_3 devices out of a single chip.

Future Work:

For future work, the Bi_2Te_3 synthesis can be refined with the goal of having fewer contaminant particulates at the moment of casting the nanorods unto the wafer. Also the selenium layer can be thinner with the intention of having a more robust device fabrication process. The back gate and top gate can be laid and impedance measurements can be done on the devices. The goal would be to produce ultra-low power transistors using a small electric field to open a gap in the surface states.

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