Fabrication and Characterization of ZnO Nanowire Field-Effect Transistors and ZnTe Nanosheet Field-Effect Transistors

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Abstract:

Zinc oxide (ZnO) is a promising material for nanodevices due to its high mobility and robust mechanical properties. The transparent nature of ZnO makes it useful for transparent and flexible electronics. Zinc telluride (ZnTe) is an easily doped direct bandgap material for optoelectronic devices. Together, ZnO and ZnTe may form a *p-n* junction, allowing the fabrication of essential electrical components such as LED's. The first focus of this project was to fabricate ZnO transistors to study the effects of low temperature fabrication process. Low temperature oxides were grown by remote plasma-enhanced chemical vapor deposition (RPEVCD) and plasma enhanced chemical vapor deposition (PECVD) for comparison with devices on thermally grown oxides. The second focus was fabricating ZnTe field-effect transistors to understand the electrical properties of nanosheets.

Introduction:

Transparent and flexible electronics have a number of exciting applications in a new generation of displays, mobile devices, and sensors. Current transparent technology uses organic materials with low mobility. ZnO is an attractive material to improve transparent and flexible technology as it is transparent, physically robust, and has high mobility to support high performance electronic applications. ZnO nanowire transistors are attractive for their high mobility and sensitivity to gas adsorption and the ultraviolet (UV) spectrum. ZnTe is an easily doped II-VI material that may potentially form a *p-n* junction with ZnO. However, realizing a II-VI *p-n* junction device requires greater knowledge of ZnTe electrical properties. This work investigated ZnTe electrical properties and low temperature ZnO transistor fabrication.

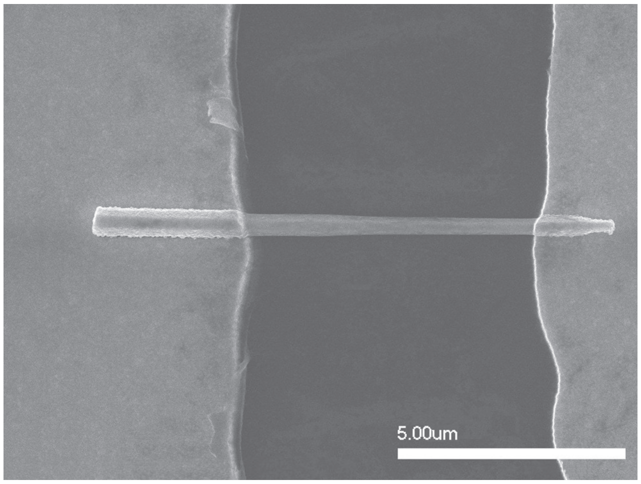
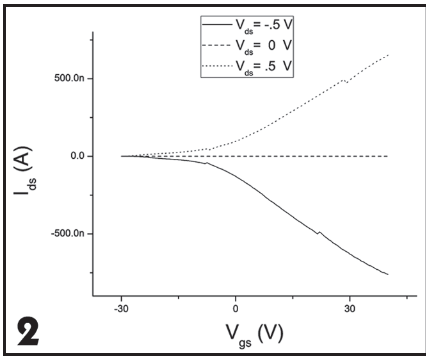


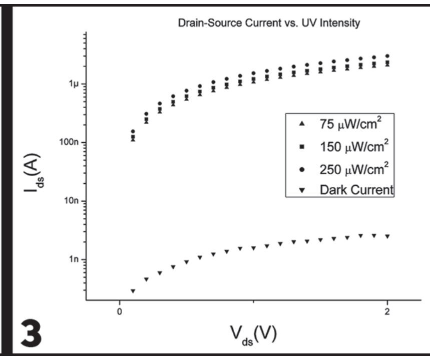
Figure 1: FESEM image of a zinc oxide nanowire transistor.

Experimental Procedure:

ZnO back-gated nanowire field-effect transistors (Figure 1) were first fabricated on 200 nm thermally grown silicon oxide (SiO_2). ZnO nanowires were grown by chemical vapor deposition (CVD) in a tube furnace with source material composed of a 1:1 ZnO and graphite mixture. Growth substrates were placed at approximately 800°C and source material was heated to 1100°C. Argon carrier gas and O_2 gas were flowed to enable carbothermal reduction of ZnO.

Growth substrates were characterized by field-emission scanning electron microscopy (FESEM), showing nanowires 5-10 μm in length with a characteristic wurtzite structure. Nanowires were transferred by mechanical slide transfer to a Si substrate with 200 nm thermally grown SiO_2. Photolithography was used to define contacts on the nanowires, and 250 nm of gold over 10 nm of chromium was deposited by thermal evaporation. ZnO nanowire current voltage characteristics were obtained with an electrical probe system. A UV lamp and meter were used to characterize the UV response of the ZnO field-effect transistors.





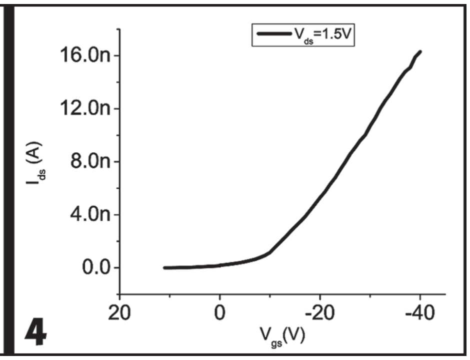


Figure 2: Zinc oxide source-drain current vs. gate bias.

Figure 3: ZnO UV response.

Figure 4: ZnTe source-drain current vs. gate voltage.

ZnTe nanosheet transistors were fabricated by similar methods, but sheets were grown at lower temperatures (approximately 600°C) with ZnTe source material. Sheets were characterized by FESEM and atomic force microscopy (AFM) showing nanosheet side lengths of 20-40 μm and a thickness of approximately 500 nm. Transfer and photolithography were performed in the same fashion as with ZnO. ZnTe nanosheet devices were characterized with an electrical probe system to determine mobility and On/Off ratios.

ZnO nanowire transistors were also fabricated on transparent glass and polyethylene napthalate (PEN) substrates. Indium tin oxide (ITO) was deposited by electron beam evaporation on silicon substrates and annealed at 135°C for eight hours in air. Low temperature oxides were grown by PECVD at 100°C and by RPECVD at 150°C. Oxides were characterized by a mercury probe system prior to transistor fabrication and nanowires were then transferred by mechanical slide transfer. Contacts were defined by photolithography and exposures were calibrated for substrate transparency. Cr/Au contacts were deposited by thermal evaporation, but in the future we hope to make the devices fully transparent using sputtered ITO contacts.

Results and Conclusions:

ZnO transistors on thermally-grown oxides were used to study the transport behavior of ZnO nanowires (Figure 2). Current-voltage characteristics showed strong *n*-type behavior. The cylinder-on-plate model was used to calculate gate capacitance, and a polynomial fit with 50 points was used to derive the transconductance of devices. A carrier mobility of 11 $cm^2/V\cdot s$ was calculated for the ZnO nanowire devices on thermally-grown oxides and On/Off ratios were approximately 10^5. Both of these parameters are comparable to other reported NWFET's [1]. The UV photoresponse of ZnO was studied by comparing transfer characteristics at variable intensities of UV radiation (Figure 3). ZnO showed a strong UV response due to its wide bandgap, as incident photons caused electron-hole pairs to form. Nanowire surface states caused the trapping of holes, providing a large photoconductive gain of 1.1×10^6.

ZnTe nanosheet transistors on thermally-grown oxide substrates also showed good performance as transistors. ZnTe nanosheet transfer characteristics showed predominately *p*-type behavior (Figure 4). Similar methods were used to calculate transconductance and gate capacitance of nanosheet devices, yielding mobility of 246 $cm^2/V\cdot s$ and a lower On/Off ratio of 103.

Successful transistor behavior was not achieved by low temperature fabrication methods. While low temperature oxides on Si substrates yielded tolerable C-V characteristics, transparent devices with 200 nm and 300 nm SiO_2 layers were found to short circuit through the gate insulator. We expect that either the inherent surface roughness of the PEN substrates or the roughness of the electron beam deposited ITO conductive back gate is the reason for this persistent problem.

Future Work:

Future work will seek to improve low temperature deposited oxide layers with low temperature annealing processes. We hope to characterize the electron beam deposited ITO conductive layer with AFM and learn how to mitigate pin-hole causing surface roughness. We hope that answering these questions will lead to flexible, transparent devices by more conventional methods than have currently been achieved.

Acknowledgments:

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References:

[1] Chang, Pai-Chun, and Jia Grace Lu. "ZnO Nanowire Field-Effect Transistors." IEEE Transactions on Electron Devices 55, no. 11: 2977-2987 (November 2008).