Fabrication of Flexible Organic Thin-Film Transistors

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Abstract:

In this work, a process for manufacturing thin-film transistors on a polyimide substrate was explored, and a novel, fast method is presented for the micro-machining of stencil masks for material deposition, with minimum opening size of 20 μm. Both *n*- and *p*-type transistors were fabricated, with the *p*-type transistors demonstrating saturation mobilities on the order of 1 cm^2/V·s, and the *n*-type transistors demonstrating saturation mobilities on the order of 0.1 cm^2/V·s. These devices can therefore be readily integrated into flexible circuits, further enabling advances in relevant technologies.

Introduction:

Several flexible materials are well-established as viable active materials for thin-film devices, such as amorphous silicon (α-Si), polycrystalline silicon, and organic materials. Organic materials are especially attractive for flexible electronics, as they have low processing temperatures that allow for compatibility with a wider range of substrates relative to other flexible materials. Organic electronics also have a demonstrated potential for low-cost mass manufacture, for instance in the form of ink-jet printing using solution-processed semiconductor materials [1].

The transistor and capacitor are two devices central to the operation of many electronic circuits. In flexible circuits specifically, the classic thin-film transistor (TFT) architecture is employed. Both capacitors and TFTs require a high-quality dielectric for successful fabrication: pinhole shorts in the dielectric render the device useless, and non-uniformity of the dielectric layer negatively impacts performance. Thus, the process for dielectric fabrication must be chosen with care.

$$f_T \propto \frac{\mu}{2\pi L^2} |V_{GS} - V_t|$$

Figure 1: Definition of transition frequency.

Experimental Procedure:

Process. The thin-film architecture employed was the traditional bottom-gate top-contact type. The fabrication process roughly followed the following procedure:

1. Spin-coat polyimide on silicon wafer as substrate
2. Deposit aluminium (Al) using stencil masked evaporation as gate layer
3. Deposit Al oxide using atomic layer deposition (ALD) as dielectric layer
4. Deposit organic semiconductor materials using stencil masked evaporation as active layer
5. Deposit gold using stencil masked evaporation as interconnection layer

Stencil Masks. The minimum opening size available in the stencil masks used determined the minimum channel length available for the transistor devices fabricated, which directly impacted the maximum speed at which the device could operate. A metric for the upper limit of operation was the transition frequency f_T, given in Figure 1. Its inverse-square dependence on length implies that small channel lengths improve the operational frequency of the device.

Mid-cost laser-cut stencil masks can achieve minimum openings around 50 μm. Micro-machined Si wafer masks can achieve opening sizes smaller than those of laser-cut masks, and thus we explored the use of deep reactive ion etching using the Bosch process to etch through Si wafers for a target minimum feature size of 20 μm. This process had a significant time advantage, as fabrication could be done in-house within a day, given the availability of a transparency mask for the photolithographic step. Externally

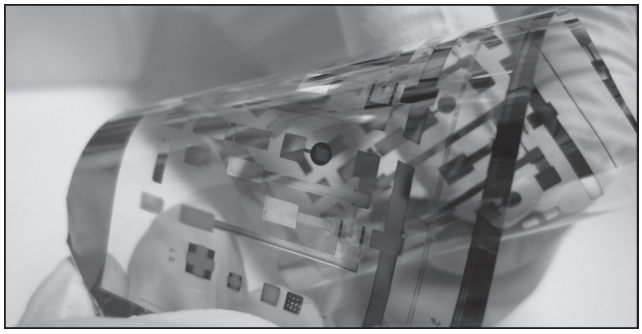

Figure 2: Fabricated devices on flexible substrate.

manufactured transparency masks have a turnaround time of 1-2 days, compared to externally manufactured laser-cut stencil masks, which may take upwards of three or four weeks to obtain.

Fabricated Devices. Using the above fabrication process, *n*- and *p*-channel TFTs were fabricated, with minimum channel lengths of 20 μm. The fabricated devices are pictured in Figure 2, and the measured V_{gs}-I_{ds} data for the devices are presented in Figure 3. The *p*-channel devices were fabricated using pentacene as the active material, and demonstrated saturation mobilities on the order of 1 $cm^2/V{\cdot}s$. The *n*-channel devices were fabricated using a perylene tetra-carboxylic di-imide (PTCDI) derivative and demonstrated saturation mobilities on the order of 0.1 $cm^2/V{\cdot}s$. These values agreed with accepted values found in literature [2].

The attained channel lengths were measured to be around 20 μm, thus validating the use of the micro-machined stencil masks. It was found that from photolithography to completed mask, the fabrication of the stencil masks took roughly five hours given the equipment available to us.

SPICE Modeling. Level 62 SPICE models for the TFTs were generated using an HSPICE optimization deck. The model I_{ds}-V_{gs} curves are presented in Figure 3. The close agreement of the models to the data support their use as models for complex circuits and allows for an initial design step before fabrication. As an example, a five-stage ring oscillator was simulated using the generated models, and the effect of channel length on frequency is demonstrated in Figure 4. A frequency of 1 kHz can be achieved at low channel lengths, highlighting the importance of small device length.

Conclusions:

We have developed a process for making both *n*- and *p*-channel thin-film transistors on a flexible substrate, polyimide. These devices exhibit performances comparable to that reported in literature. The minimum device size of these devices was approximately 20 μm, enabled by micro-machined silicon masks. The simplicity of the process as well as the fast turnaround time of the masks allowed for reasonably fast fabrication in an academic setting. Because both *n*- and *p*-channel devices were available, this process can be used to fabricate digital circuits using a complementary design. Future work will involve fabrication of digital integrated circuits using this process for mounting on curved surfaces.

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References:

[1] Minemawari, H., Yamada, T., et al. "Inkjet printing of single-crystal films"; Nature 475, 365-367 (2011).

[2] Bao, Z. and Locklin, J.. Organic FETs. CRC Press, 2007.

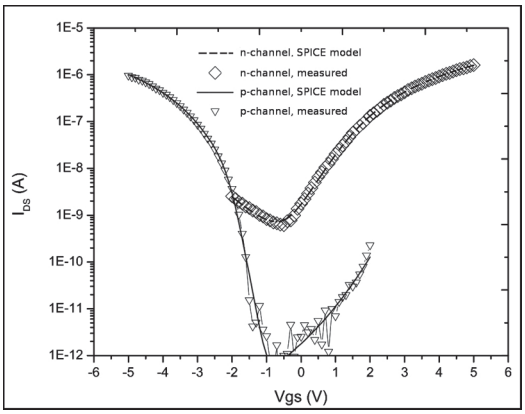

Figure 3, above: V_{gs}-I_{ds} curves for fabricated devices and for constructed device models.

Figure 4, below: Simulated frequency of five-stage ring oscillator as function of device channel length.