Metal Nanocrystal Nonvolatile TFT Memory Cells

Ravneet Bajwa
Electrical Engineering and Computer Science, University of California, Berkeley

NNIN REU Site: Cornell NanoScale Science & Technology Facility, Cornell University
NNIN REU Principal Investigator: Dr. Edwin Kan, Electrical and Computer Engineering, Cornell University
NNIN REU Mentors: Jaegoo Lee and Alex Tou-Hung Hou, Electrical and Computer Engineering, Cornell University
Contact: raybajwa@berkeley.edu, kan@ece.conell.edu

Abstract:

Nonvolatile memory cells consisting of a heterogeneous self-assembled gold nanocrystal floating gate and ultra thin gate oxide were fabricated in the thin film transistor (TFT) level. The memory cells are designed to be used in flash memory applications and to improve the conventional design in terms of higher packing density, faster program/erase (P/E) operation and lower operational voltage. To achieve a controllable thin body layer, a chemical mechanical planarization (CMP) process for polysilicon was established. It was important to achieve this so that the charge stored in the gate stack layer could effectively control the channel conductance, instead of being dominated by the traps in the grain boundaries. Subsequently, the rest of the process—ultra thin oxide growth, self assembled gold nanocrystal formation, oxide and chromium deposition—was completed. In upcoming days, the devices would be characterized by measuring the memory window, P/E voltage, P/E time, retention time and cycling endurance.

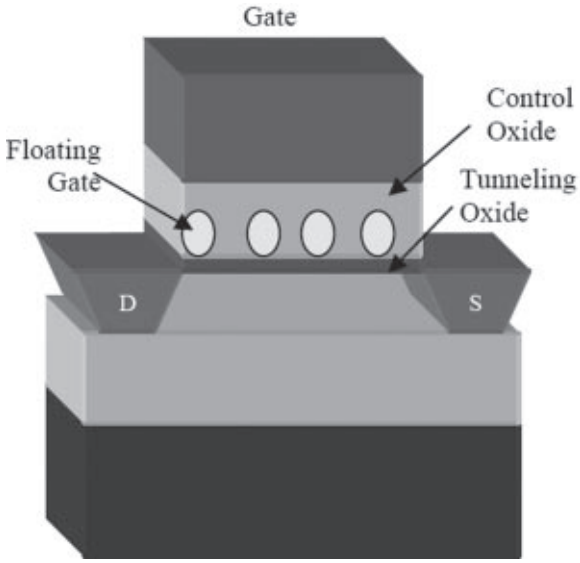

Figure 1: Structure of a memory cell.

Introduction:

Figure 1 shows the structure of the metal nanocrystal nonvolatile memory cell. By applying a high voltage across the gate, electrons are forced to quantum mechanically tunnel through the thin oxide and deposit charge on the floating gate. Depending on the amount of charge on the floating gate, the threshold voltage of the device varies. Two such states with sufficiently large threshold voltage difference, known as memory window, can therefore be used to represent the binary logical states. Currently, there are two major limitations in the conventional memory cell design: program/erase (P/E) operation takes considerably long (1-10 ms) and P/E voltage is too high (12-19V). These could however be improved if the tunneling oxide thickness is reduced but the scaling down of the existing design is limited due to high leakage current which degrades the retention characteristics. Thus, an improvement in the design is needed. This project was aimed at fabricating and characterizing an improved design with two major distinctions: using gold nanocrystals as a discrete floating gate which would reduce the leakage current as oxide thickness is reduced, and using thin polysilicon film as the transistor substrate which would enable 3-D integration of memory cells and provide compact embedded memory for devices.

Experimental Procedure:

The first step of the fabrication process was to obtain about 20 nm thick polysilicon film with RMS roughness below 2 nm. To achieve this we had to establish a CMP process using the Strasbaugh 6EC CMP tool.

A two-level four-variable statistically designed experiment was thus set up. The four variables (values chosen) under testing were: down force (4 and 6 psi), table speed (15 and 25 rpm), chuck speed (15 and 20 rpm), and slurry type (Semi-Sperse® P1000 and Semi-Sperse® 12). The thickness and roughness of the wafers were measured before and after the CMP process, and the

removal rate for each setting was calculated. The settings were then compared to choose the best combination. After establishing this process, fabrication of our device wafers was started.

About 500 nm of PECVD oxide was deposited on a silicon wafer which was followed by a 100 nm undoped polysilicon deposition. This polysilicon was then polished down to about 20 nm by using the established CMP process. The next step was to grow 3 nm of oxide and it was followed by about 1.2 nm of gold deposition. The gold self-assembled into nanocrystals (6 nm in diameter) owing to high surface energy difference.

Next, about 30 nm PECVD oxide was deposited and finally 200 nm of chromium was evaporated on the wafer to serve as the gate electrode.

Results and Conclusions:

The first interesting fact learned while establishing the CMP process was that native oxide grown on polysilicon, even a few angstroms, considerably reduced the overall removal rate when P-1000 slurry was used. Consequently, the process was adapted by adding a HF dip step to remove the native oxide immediately before polishing the wafers, thus making the CMP process more predictable. Removal rate and uniformity of different settings used in the design of experiment (DOE) are summarized in Table 1 and 2. Clearly, setting 4 had the least removal rate and most uniformity. Also, as shown in Figure 2, AFM roughness results revealed that RMS roughness of polysilicon decreased down to an acceptable value of 1.29 nm from about 4.05 nm and therefore this setting was chosen. Using this setting, smooth polysilicon films as thin as 15 nm were successfully obtained and processed further to make devices. Finally, the wafers were sent out for ion implantation to enhance the conductivity of the drain and the source terminals.

#	Down force / Table speed / Chuck speed (psi /rpm /rpm)	Removal in 45s (nm)	Standard Dev.
1	6/ 25/ 15	109.3	30.7
2	4/ 25/ 25	86.1	10.4
3	6/ 15/ 25	112.9	11.0
4	4/ 15/ 15	74.4	8.2

Table 1, above: CMP data using P-100 slurry.

Table 2, below: CMP data using SS-12 slurry.

#	Down force / Table speed / Chuck speed (psi /rpm /rpm)	Removal in 45s (nm)	Standard Dev.
5	6/ 25/ 25	162.1	16.3
6	4/ 25/ 15	115.0	12.7
7	6/ 15/ 15	127.9	20.3
8	4/ 15/ 25	73.7	18.3

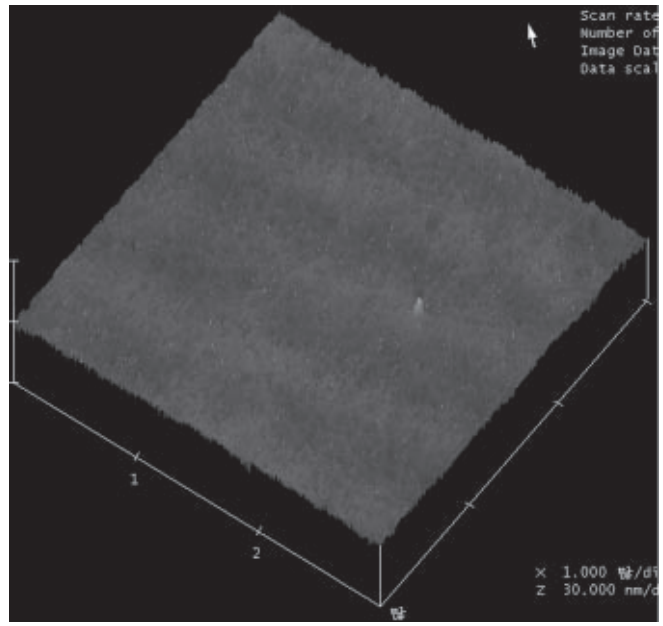

Figure 2: AFM image of polished polysilicon.

Future Work:

The devices will soon be characterized by measuring the memory window, P/E voltage, P/E time, retention time and cycling endurance. The design will then be optimized until we meet our goals of faster and low power-consuming flash memory.

Acknowledgements:

This study was funded by NSF through National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program at Cornell NanoScale Facility, Cornell University. I would like to thank Dr. Edwin Kan, Jaegoo Lee, Alex Tou-Hung Hou, CNF staff, and the rest of the Kan group.